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Baseband Analog Circuits for Software Defined Radio

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BASEBAND ANALOG CIRCUITS
FOR SOFTWARE DEFINED RADIO

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Baseband Analog Circuits for Software Defined Radio

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A mamma, papà, Carmelo e Luca perché so di poter sempre contare su di loro.

To Beatriz and our sweetest baby girl, Sofia Melina, for their love, trust and constant support.

Contents

Preface

WITH the rapid development of wireless communication networks, it is expected that fourth-generation (4G) mobile systems will appear in the market by the end of this decade. These systems will aim at seamlessly integrating the existing wireless technologies on a single handset: together with the traditional power/size/price limitations, the mobile terminal should now comply with a multitude of wireless standards. Software Defined Radio (SDR) can be the right answer to this technology demand. By restricting the meaning of the term SDR to the analog world, we refer to a transceiver whose key performances are defined by software and which supports multistandard reception by tuning to any carrier frequency and by selecting any channel bandwidth (Abidi, 2006). In the future, SDR might become a "full digital" Software Radio (SR) (Mitola, 1995, 1999) where the digitization is close to the antenna and most of the processing is performed by a high-speed Digital Signal Processor (DSP). Though, at present, the original SR idea is far ahead of state of the art, mainly because it would demand unrealistic performance for the Analog to Digital Converter (ADC).

We believe that a fully reconfigurable Zero-IF architecture that exploits extensive migration toward digitally assisted analog blocks (Craninckx et al., 2007) is the best candidate to realize a SDR front end as it has the highest potential to reduce costs, size, and power, even under flexibility constraints. Although this solution itself does not allow simultaneous reception of more than one channel, two parallel front ends of this kind would cover most of the user needs, while still allowing cost saving compared to parallel single-mode radios.

The objective of this book is to describe the transition towards a SDR from the analog design perspective. Most of the existent front-end architectures are explored from the flexibility point of view. A complete overview of the actual state of the art for reconfigurable transceivers is given in detail, focusing on the challenges imposed by flexibility in analog design. As far as the design of adaptive analog circuits is concerned, specifications like bandwidth, gain, noise,

resolution, and linearity should be programmable. The development of circuit topologies and architectures that can be easily reconfigured while providing a near optimal power/performance trade-off is a key challenge. The goal of this book is to provide flexibility solutions for analog circuits that allow baseband analog circuits to be part of an SDR front end architecture. In more detail, there are two main features that need to be implemented:

- **Performance reconfigurability.** This allows compatibility with a wide range of wireless standards. In analog words, that means that parameters such as cut-off frequency, selectivity, noise, and linearity for the filter, gain, and bandwidth for the amplifier, number of bits, and sampling frequency for the ADC, should be digitally programmable.

- **Energy scalability.** Let us assume that the task is to transmit a packet of L bytes. Suppose that the considered system can proceed to that transmission at a rate R byte/s with a power PW or at rate $(R/2)$ byte/s with power $(2P/3)$ W. This is hence a power manageable component since a lower performance leads to a lower energy per bit (Bougard, 2006).

The challenge is then to provide at any time the best power consumption vs performance trade-off. It is clear that analog reconfigurability may come at the cost of power, silicon area, and complexity. Therefore, one of the goals is to try to minimize such costs. We will have to deal with many cross-disciplinary aspects which are the key to a good-enough analog design with reduced die size, power consumption, and time-to-market. They will be emphasized at all design steps, from defining requirements at first, to deriving specifications through end-to-end system simulation, and finally global verifications.

The book is structured as follows:

- **Chapter 1** discusses the benefits and the enormous challenges of migrating to fourth generation (4G) mobile systems focusing on the mobile handset. The role of analog circuits is identified and a possible platform for the mobile terminal is proposed.

- **Chapter 2** investigates a number of architectural issues and trade-offs involved in the design of analog transceivers for a fully integrated multi-standard SDR. After commenting on the state of the art for SDR front end integrated circuits, a flexible zero-IF architecture for SDR is suggested, supported by implementation and measurements results.

- **Chapter 3** discusses the practical aspects that have to be taken into account when the specifications for an SDR must be derived. The optimal specifications distribution for minimum power consumption is given focusing on the baseband section.

- **Chapter 4** comments on the challenges that analog design for flexibility imposes to a designer and shows a possible way to tackle them. Basic flexible analog building blocks are then analyzed from the flexibility perspective trying to figure out an optimal implementation.

- **Chapter 5** shows two possible implementations of flexible baseband analog sections. The implementations are described and measurements results prove the validity of the proposed approaches.

Finally, this book is the result of a Ph.D. research work and, as such, it comes out of years of readings, study, and hard work. We do realize that it could be definitely improved as errors or omissions may easily occur in works of this kind. Many of the analog techniques described in the book have already been published in the past and references are carefully reported so that the reader can eventually further delve into the topic. We would strongly appreciate if you could bring your opinion to our attention so that eventual future editions can be improved.

VITO GIANNINI

Acknowledgments

Chapter 1

4G MOBILE TERMINALS

WITH the rapid development of wireless communication networks, it is expected that 4G mobile systems will be sent to market by the end of this decade. While third-generation (3G) mobile systems focused on developing new standards and hardware, their 4G evolution will aim at seamlessly integrating the existing wireless technologies (Hui and Yeung, 2003). Fourth-generation systems will support comprehensive and personalized services, providing not only high-quality multimedia and broadband connectivity, but also high usability (wireless connection anytime and anywhere). However, migrating current systems to 4G presents enormous challenges and, in particular, the design of the mobile terminal represents the real bottleneck because of the concurrent power/performance/price limitations that a base station does not have (De Man, 2005). This chapter will discuss these challenges.

1.1   A Wireless-Centric World

Since Nikola Tesla, in 1893, carried his first experiments with high-frequency electric currents and publicly demonstrated the principles of radio broadcasting, society witnessed so many changes in which that discovery had an important role. Wireless communication has become incredibly essential in today's world. Whether we will want it or not, wireless devices will have, increasingly, a significant impact in our everyday life.

In the close future, a smart wireless device able to provide information, communication, and entertainment could be in the pockets of millions of users. This Universal Personal Assistant (UPA) will be powered by battery or fuel cell (De Man, 2005). In the business environment, it would serve the purpose of mobile computing, wideband ubiquitous communication, and audio/video conferencing. High-speed data links will be provided by Wireless Local Area

Network (WLAN), but only in the home of office environments and at a number of hot spots, e.g. in airports. Global coverage for connection to the rest of the world happens over the radio access link of a cellular or satellite network. For example, in our cars, it would lead to security improvements and intelligent navigation. The entertainment industry could propose new advanced gaming services usable anywhere. The mobile terminal could become a real-time health wireless monitor, where body temperature, heart rate, and blood pressure could be checked anytime for high-risk individuals still allowing them to live a normal life. A high level on encryption and new advances in cryptography might enable the use of electronic cash by simply pushing a button on a mobile handset, which could also allow access to its owners to create wireless keys for homes, cars, and safes. Finally, governments could allow the use of wireless identification devices. All this culminates in the vision of Ambient Intelligence (AmI), a vision of a world in which the environment is sensitive, adaptive, and responsive to the presence of people and objects (Boekhorst, 2002) and the user is able to interact at several levels with several objects.

Typically, this AmI vision involves discussions at very different levels: from more technical details to ethics and privacy issues. Focusing on the technology challenges, what is clear is that to enable this vision two things will be essential:

- A Wireless Sensors Network (WSN)

- A Smart Reconfigurable Wireless Terminal

While several universities and research centers are actively working on WSN, the idea to develop a smart wireless terminal is already at more advanced stages forced by the strong demand for highly flexible transceivers. The proliferation of mobile standards and the mobile networks evolution make the global roaming and multiple standard compliancy a must for a modern terminal. The problem of integrating more radios on a single terminal involves discussions on performance, that has to be good enough to receive different modulations, carrier frequencies, and bandwidths. Power consumption is critical for such devices, where the need of tougher performance contrasts with the always actual problem of extending the battery life as long as possible. In addition to that, the number of components on a single terminal might have an impact on the size/cost of the final wireless product. In this context, the possibility to reduce the number of components on a single mobile terminal by integrating different radios on a single radio Integrated Circuit (IC) could indeed allow cost savings while still guaranteeing optimal power/perfomance/cost trade-offs.

If we wanted to put the vision previously described in terms of wireless standard needed for a certain application, we would realize how it is actually very difficult to have a single terminal able to work for such a wide range of services. While voice digital broadcasting requires high mobility at low data rates, a video phone call needs devices compliant with data rates as high as
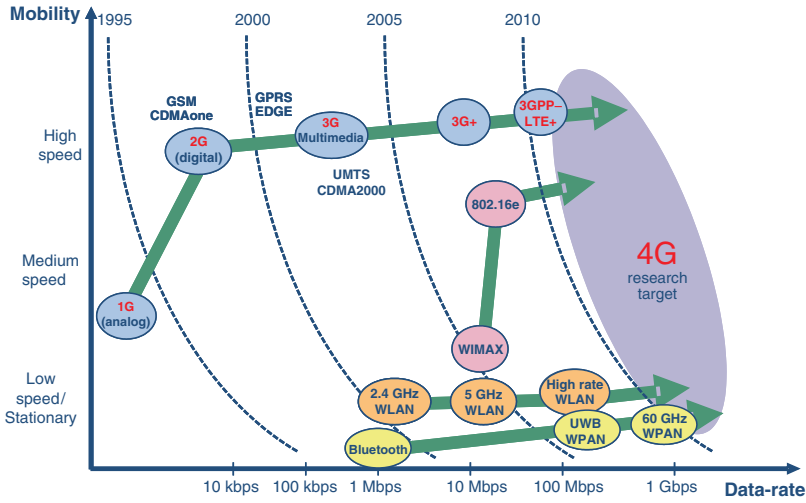
Figure 1.1.   Plethora of emerging and legacy wireless standards.

100 Mb/s. Finally, low data rate control signals that form the interface between environment and system with data rates as low as 100 Kb/s (i.e. a wireless health monitor) might require a Wireless Personal Area Network (WPAN), and so low mobility, wide band, and even tougher power constraints. Figure 1.1 shows a compact picture of the evolution of the wireless standard versus the mobility/data rates requirements.

Energy-efficient platforms are needed that can be adapted to new standards and applications, preferably by loading new embedded system software, or by fast incremental modifications to obtain derived products. This might be possible by exploiting the intrinsic capabilities offered by CMOS deep sub-micron processes.

1.2   The Driving Forces Towards 4G Systems

Since mobile phones began to proliferate in the early 1980s with the introduction of cellular networks many steps have been done. The success of second-generation (2G) systems such as GSM and CDMA in the 1990s prompted the development of their wider bandwidth evolution. While 2G systems were designed to carry speech and low-bit-rate data, 3G systems were designed to provide higher-data-rate services. Figure 1.2 shows this technology evolution: a range of wireless systems, including GPRS, EDGE, Bluetooth, and WLAN, have been developed in the last years that provide different kind of services. All these systems were designed independently, targeting different service types, data rates, and users. As these systems all have their own merits and short-comings, there is no single system that is good enough to replace all the other
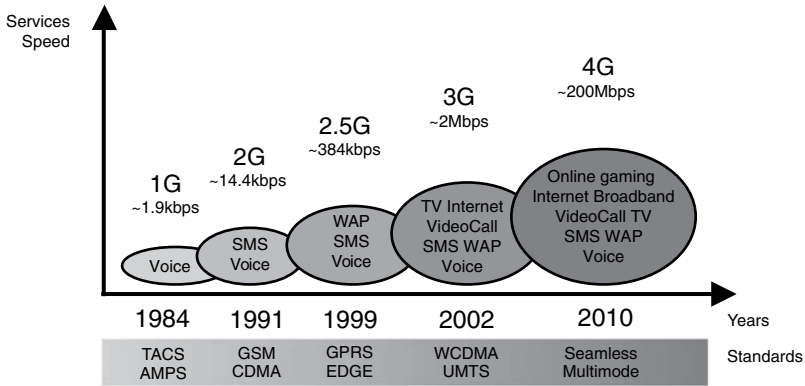
Figure 1.2. Short history of mobile telephone technologies.

technologies. Driven by the enormous success of the Internet over the last 10 years, with steadily increasing data rates and deployment of new services, extra expectations have emerged. Not only traveling businessmen and executives, who were already the early adopters of cellular communications, but the wide majority of mobile users demand for low-cost connectivity while on the move (Zanariadis, 2004). Instead of putting efforts into developing new radio interfaces and technologies for 4G systems, we believe establishing 4G systems that integrate existing and newly developed wireless systems is a more feasible option.

The following requirements for a 4G terminal are identified as important drivers for the research on the mobile terminal:

- **High usability.** 4G networks are all-IP based heterogeneous networks that allow users to use any service at any time and anywhere. Low-cost ubiquitous presence of all broadcast services, with bit rates comparable to those offered by wired systems, forms a compelling package for the end user and can truly make the mobile terminal a centrepiece of people's lives. Ubiquitous coverage is a key feature to have an impact on the market because users might not be willing to renounce to the fine coverage of the Global System for Mobile Communication (GSM) services in favor of more advanced but poorly available (at least in the early stages of development) wireless networks. Therefore, it is essential to develop an architecture that is scalable and can cover large geographical areas and adapt to various radio environments with highly scalable bit rates, while encompassing the personal space (BAN/PAN) for virtual reality at faraway places.

- **High-quality multimedia.** *Video conferencing* is an essential part of the mobile terminal. Having an autonomy for at least 1 h, of full high-quality video conferencing with four participants is strategic for the proliferation

of such a device. *Autonomous movie watching* is also a basic requirement: 2 h of high-quality movies and 10 h of low-quality movies. *Advanced gaming* will be common on the mobile terminal, so it is required to have 10 h online high-quality gaming with a minimum players of 16 with support for multiplatform gaming.

- **Multiband/broadband connectivity.** Peak speeds of more than 100 Mbps in stationary mode with an average of 20 Mbps when traveling are expected. Currently, we see the following standards play an important role in such a multimode terminal: Bluetooth, Zigbee, Universal Mobile Telecommunications System (UMTS), WLAN (moderate throughput 802.11a physical layer + 802.11e Media Access Control (MAC) centralized/high throughput 802.11n physical layer Multiple-Input Multiple-Output (MIMO) + MAC centralized), Worldwide Interoperability for Microwave Access (WiMAX), Digital Video Broadcasting-Handhelds (DVB-H)/UMTS combined modes, 802.15 Body Area Networks (BAN), WPAN, Global Positioning System (GPS), Digital Audio Broadcasting (DAB).

- **Service personalization.** Future communication systems will provide the intelligence required for modeling the communication space of each individual. The future service architecture will be I-centric (Tafazolli, 2004). I-centric communication considers human behavior as a starting point by which to adapt the activities of communication systems. Human beings do not want to employ technology but rather to interact with their environment. They communicate with objects in their environment in a certain context. In this context, personalized services will be provided by this new-generation network.

A number of marketing studies show that size, cosmetic appearance, weight, and battery life are the main factors that influence a consumer in purchasing a new mobile phone. Therefore, the key of the commercial success of the 4G handset will be the number of supported features offered at minimum power consumption and cost, as well as the efforts by service providers to design personal and highly customized services for their users.

Figure 1.3 shows the current view on what a 4G wireless terminal should look like. The user should be able to access services and information at home, walking in urban areas, driving his car, driving to work, and even in more desolated areas. We will communicate over varying distances and varying bit rates with a broad range of applications and persons. IPv6 (Internet Protocol version 6) will lead to an increase in the number of addresses available for networked devices, allowing, for example, each mobile phone and mobile electronic device to have its own IP address. The air interface we will use will depend on the instantaneous requirements: low-power, low-data rate systems
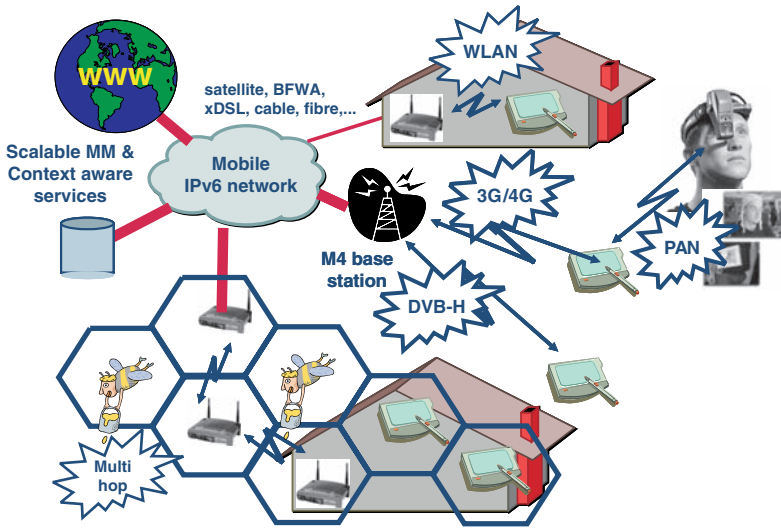
Figure 1.3.   A view of the ubiquitous network of the future.

for the WPAN, global coverage and medium data rates for cellular systems, local coverage and high data rates for WLAN. The wireless terminal should be compliant to all (or a large subset of) current existing standards to provide backwards compatibility. New air interfaces might be developed that employ reconfigurable coding and modulation schemes and multiantenna techniques that adapt to the circumstances to provide optimal communication. The limitations of a certain air interface and the transitions between them should be transparent for the user. In a heterogeneous environment such as the one that 4G terminals require, conditions are much more varying than in a more fixed environment. A high-quality terminal should be able to handle those changes in environmental conditions, and offer the best quality of experience for the user. In addition to that, the mobile terminal market is highly competitive with mass market products. As a consequence, the lifetime of such terminal will be short, and time-to-market pressures are enormous.

1.3   Basic Architecture For a 4G Terminal

In order to use the large variety of services and wireless networks in 4G systems, multimode multiband wireless handsets devices terminals are essential as they can adapt to different wireless networks by reconfiguring themselves. This would eliminate the need to use multiple terminals (or multiple hardware components in a terminal).

The most promising way of implementing multimode terminals is to adopt the Software Defined Radio (SDR) approach with multiple-antenna (MIMO)
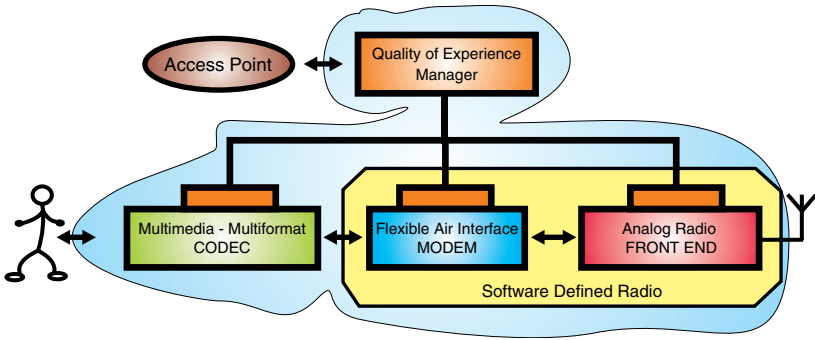
Figure 1.4. Possible basic architecture of a 4G terminal, developed for the M4 program at IMEC.

techniques for bandwidths in excess of 100 Mbps. SDR enables multistandard reception by tuning to any frequency band, by selecting any channel bandwidth, and by receiving any known modulation (Abidi, 2006). In the future, SDR might become a "full digital" SR (Mitola, 1995, 1999) where the digitization is close to the antenna and most of the processing is performed by a high-speed DSP (Tuttlebee, 2002; Bose et al., 1999; Lackey and Upmal, 1995). Though, at present, the original SR idea is far ahead of state of the art, mainly because it would demand unrealistic performance for the Analog to Digital Converter (ADC). In the last few years, several attempts have been made in the SDR direction based on different architectures (Bagheri et al., 2006; Muhammad et al., 2006; Karvonen et al., 2006; Liscidini et al., 2006).

The main target for a SDR front end is to reduce the radio cost by a factor of 2 by sharing hardware (Craninckx and Donnay, 2003). A first estimate shows that the cost for a radio front end that supports several standard by duplicating the hardware will be prohibitive and will be a roadblock for introduction of the 4G terminal in the broader market. Figure 1.4 shows our idea of *4G mobile terminal*. Because of the many wireless existing standards and the ones still in development, the RF front end and Air Interface of the multimode terminal must become very flexible. This is the only way to implement all the identified modes in a cost-effective way, and to ensure that new modes can be added with minimized time-to-market. The RF front end should be flexible and controllable from a power perspective and the FLexible Air Interface (FLAI) should enable high spectral efficiency solutions. The *Multimedia Multiformat* (3MF) CODEC block should support audio and video compression standards as well as 3D graphics standards. The idea is to develop a flexible heterogeneous platform that can support contemporary and emerging video and audio compression standards and will demonstrate a power-efficient implementation of the emerging Scalable Video Coding (SVC) standard on the heterogeneous

platform. The SVC seems to be the best multimedia compression technique to deal with multimedia applications in a dynamic and changing environment. Finally, nowadays wireless terminals are typically designed for worst-case conditions. This comes with an enormous energy penalty. Exploiting the dynamism in the channel conditions and application requirements can lead to enormous power reductions. An intelligent controller will link application, transmission and terminal resources in order to optimize the *Quality of Experience* for the user (QoE).

1.4   The Role of Analog Circuits

The mobile terminal represents the real bottleneck to make the wireless centric world a reality. The power/performance/price limitations on the mobile terminal force indeed trade-offs that a base station does not have and these limitations of handsets currently dictate inflexible networks. While analog designers squeeze every dollar and every dB out of their front ends, they are sliding down a curve of diminishing returns. The future of wireless semiconductors and the road to connectivity utopia lies in all-CMOS radios with agile-RF front ends and SR architectures. The RF section will become a smaller and smaller piece of the overall pie. That is why some researchers are trying to reduce cost, power, and board area through the use of a digital RF front end based on a sampled data converter with switched-capacitor filtering. The goal is to directly digitize the RF signal to eliminate the analog and mixed-signal circuitry typically required between the RF and baseband. Though, for several reasons, this is not a realistic scenario. Let us make an example: assuming 900 MHz as carrier frequency for a direct conversion receiver, according to the Nyquist's theorem, our software radio must operate at least at 1.8 Gs/s. If our processor runs at 4 GHz and it can perform four operations per cycle, assuming that the software radio algorithms provide 100% utilization of the CPU and memory, our theoretical device performs 16 Giga operations per second. At a sample rate of 1.8 Gs/s, that means this hypothetical device can perform about eight operations per sample. This is not enough to implement any sort of realistic radio. In addition to that, modern DSPs, which are rated at 4 Giga operations per second have a power dissipation that a modern battery cannot afford.

Therefore, it is more accurate to say that the future of wireless semiconductors lies in continued optimization of tools, devices, architectures, software, and overall systems to meet the power, cost, performance, size, processing, and time-to-market requirements of 4G wireless devices. In this context, analog signal processing is still necessary and, at the moment, using an analog front end seems to be the only feasible way to really implement an, SDR. If, in the previous example, we used analog filters for some of the initial receiver stages and operate the SR at lower frequencies, we would have more headroom to
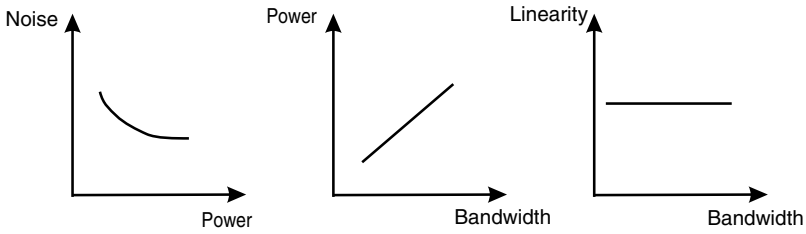
Figure 1.5. Power/performance trade-offs on a scalable analog circuit.

perform useful work on operations. But that also makes the radio somewhat less flexible.

The problem is then shifted: it is no longer a matter of whether or not to use analog circuits, but, instead, the problem is to add somehow several degrees of freedom to analog circuits so enabling the level of flexibility required by an SDR. The idea is to make every analog block reconfigurable and to tune its performance by programming knobs by means of digital interfaces. "Clean" analog designs are needed that are reconfigurable without giving in on actual performance, and allow making a trade-off between typical specs such as gain, noise, linearity, bandwidth, and certainly also power consumption (Figure 1.5).

1.5 Energy-Scalable Radio Front End

Sharing the hardware by using novel circuit techniques and advanced RF technologies can bring the cost for the radio front end to an acceptable level. While optimizing individual blocks in terms of power consumption and space is one route to mitigating the impact of multiple RF chains, other paths exist to achieve that optimization. The SDR front end is a versatile platform which provides interoperability by connecting modularized and flexible hardware building blocks and by defining tasks at a software level. Figure 1.6 shows a basic block scheme for the overall analog front end: the basic architecture includes an antenna, the RF analog transceiver, ADC and Digital to Analog Converter (DAC), the Air Interface and the digital interconnection.

- **SDR antenna interface**. The signal conditioning starts already at the antenna and several blocks are already needed at this level. Because of the different blocking levels the receiver needs to cope with, RF band-select filtering is needed between the antenna and the Low-Noise Amplifier (LNA). In addition to that, a TX/RX switch diplexer, matching components for the LNA input, Power Pre-Amplifier (PPA) and PA outputs are normally needed. They will all have to provide flexible features. Therefore, they could be integrated on a Deposited Multi-Chip Module (MCM-D) (either on glass or on high silicon) with lumped elements, transmission lines, and
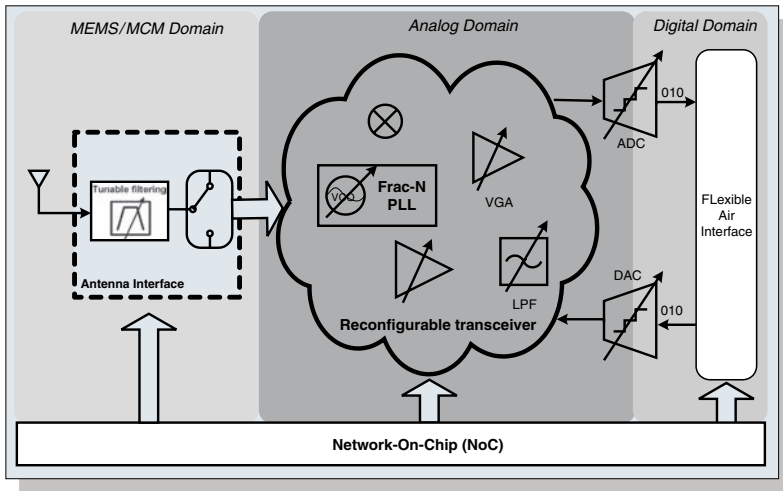
Figure 1.6. The SDR analog front end is made of an intelligent antenna interface designed in MEMS technology, an analog programmable CMOS transceiver, high-performance low-power ADC and DAC and a flexible interface. The different blocks communicate with each other with a fast NoC.

MEMS components (e.g. switches for large frequency variations and varicaps for fine-tuning) (Innocent, 2004; Spengen, 2004). The MEMS use the electrically controlled movement of a cantilevered arm to modify the values of capacitive and inductive filter components. They can also be used to change the matching for antennas. The devices can change the characteristics of a filter within a millisecond and have the additional advantage of being almost a perfect wire, so there are no losses associated with them. Reliability remains a question, as do size and cost. Nonetheless, many researchers are confident that MEMS are one of the keys to unlocking agile RF front ends (Tilmans et al., 2003; Nguyen, 2006).

- **SDR analog front end**. To participate to power saving on the average and reach this goal, the analog front end should adapt its performances (and power consumption) to the changing link requirements (user) and conditions (channel) and on the average. Power consumption obviously needs to be constrained and even dynamically minimized to bring the battery lifetime to an acceptable level. However, flexibility comes at the cost of complexity and extra power, and the front end in each specific mode should not exceed (too much) the power consumption of one single-mode radio. The RF and baseband building blocks should be reconfigurable in performances (channel bandwidth and center frequency, noise, gain, linearity, etc.) and power consumption. More details on the possible options for implementing a SDR analog front end will be given in the following chapter.

■ **SDR digital baseband engine**. Also in the design of reconfigurable digital baseband engines, flexibility has to be carefully traded off with energy efficiency. Assuming that 100 MOPS/mW is an acceptable energy efficiency for a mobile handset, we soon realize that the flexibility offered by fine-grained adaptive algorithms and implementations may be more efficient than fixed nonadaptive hardware solutions. This comes from the fact that these flexible solutions have the potential to continuously adapt to the environment and application dynamics for energy savings. Most of the present processor architectures intended for a SDR modem are designed based on the specific Physical Layer (PHY) signal processing algorithm in the wireless standard. The final architecture results in a smart combination between fine and coarse-grained reconfigurable arrays (FGAs and CGAs) and very long instruction word (VLIW) solutions (Dejonghe et al., 2007).

1.6 Towards Cognitive Radios

Besides the energy constraint, spectrum is also becoming a major bottleneck for the future wireless terminals. The concept of Cognitive Radio (CR) includes the research of new paradigms for efficiently exploiting the available spectrum. A smart device will be able to analyze the radio environment and decide for itself the best spectral band and protocol to reach whatever base station it needs to communicate with, at the lowest power consumption possible (Rubenstein, 2007). Standardization is currently ongoing in the IEEE 802.22 working group. The spectrum sensing and agile air interface requirements of CR call for SDR-based implementations. However, deciding which portion of the spectrum to use at any given moment is only one of the aspects of what CR could do: together with a WSN, it will indeed be the real enabler of the wireless centric world previously described.

Chapter 2

SOFTWARE DEFINED RADIO FRONT ENDS

D URING the last 10 years, the idea of Software Defined Radio (SDR) gained momentum pushed by the need of a wireless multistandard radio terminal capable of operating according to a variety of different mobile communication standards. Starting from the ideal concept of Software Radio (SR), this chapter investigates a number of architectural issues and trade-offs involved in the design of a fully integrated multistandard SDR front end. Receiver configurations such as heterodyne, zero-IF, digital low-IF, bandpass sampling, and direct RF sampling are described from the flexibility perspective. The state of the art for SDR front ends IC is given commenting different solutions proposed in the last years. An SDR front end based on a zero-IF receiver, which is the reference architecture for the rest of this book, is described in detail. To end the chapter, digital calibration techniques are shown that compensate for different analog imperfections in direct conversion transceivers.

2.1   The Software Radio Architecture

Software Radio (SR) is a sophisticated radio that uses software to create high-performance, flexible communication devices performing digitally most of the signal processing tasks that analog circuits traditionally handle. It offers the advantage of putting many traditionally inflexible features in modules whose characteristics can be changed while the radio is running (Wolf, 2005). For example, rather than design a single radio to receive only a certain carrier frequency, bandwidth, and modulation as defined by the wireless standard, engineers could program a very flexible digital transceiver to provide receiving capabilities over a wide range of frequencies while the radio operates.
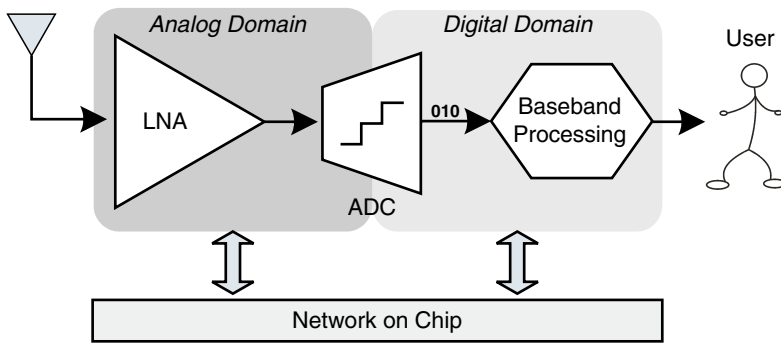
Figure 2.1.   The ideal software radio architecture exploits a performing ADC almost at the antenna and moves most of the RF typical functions to the digital domain.

The ideal SR architecture is shown in Figure 2.1, as proposed by Mitola (1995, 1999). This receiver allows simultaneous reception of every channel incident on the antenna. The only analog components are a reconfigurable antenna and a high dynamic range LNA with built-in Automatic Gain Control (AGC). Analog-to-digital conversion is done immediately at RF in order to digitally elaborate the signal on a flexible air interface. Downconversion and filtering operations are performed by a reprogrammable baseband DSP. The DSP processes the digitized signal in accordance with the wireless environment.

A good example of ideal SR transceiver is a prototype designed by the UK Defence Agency for High Frequency (HF) applications (Davies, 2000). Military communications may strongly benefit by using SR transceiver and therefore digitize and demodulate the entire bandwidth of interest. By digitally downconverting and filtering every channel in the band, a single ADC enables simultaneous reception of anything present in the air at that very moment. Full integration is still possible because the range of frequencies of interest, in this case from 3 to 30 MHz, require a 12 bits, 75 MHz A/D converter, which is state of the art. The ADC is placed early in the signal path, using afterwards a DSP for channel selection and demodulation. Yet, an Low-Pass Filter (LPF) is required before the conversion to the digital domain to avoid aliasing and limit the ADC resolution. The potential benefits of this architecture include reduced complexity, lower components count, simultaneous reception of multiple channels, reconfigurability, and some performance advantages.

Unfortunately, this SR architecture cannot be extended further than those range of frequencies nowadays. This is due mainly to the following technological limitations:

- It is very difficult to implement just one antenna and one LNA to serve a bandwidth ranging from hundreds of megahertz to several gigahertz (i.e. to cover the bands of all 4G wireless networks, Figure 2.2). With the available
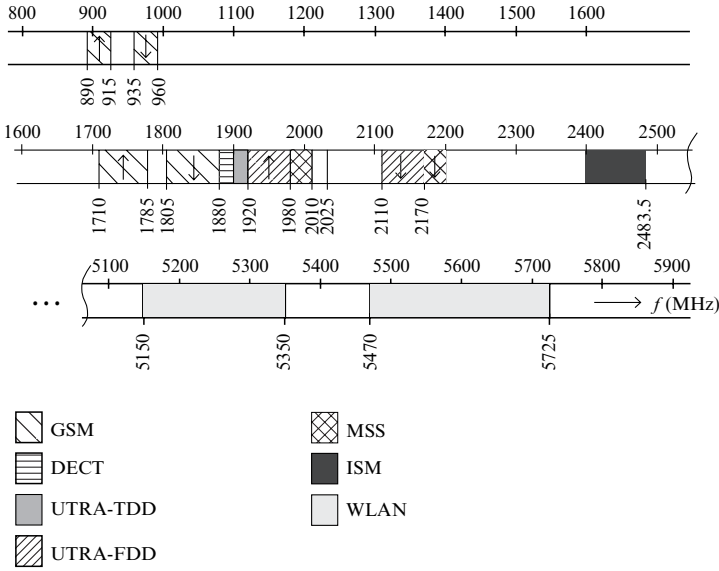
Figure 2.2. Mobile spectrum in Europe. (From Jondral, 1999.)

technologies nowadays, the only solution is to use multiple analog parts to work in different frequency bands. This certainly increases the design complexity and physical size of a terminal.

- Existing ADC performance still is not sufficient enough to perform digitization of all the present wireless standards at RF. Particularly, the analog input bandwidth, sampling rate, dynamic range, and therefore resolution need considerable amounts of technology improvements if wideband front end and sampling at RF are to become reality. Let us take an example: according to the Nyquist theorem, the highest carrier frequency that can be received by an ideal SR is limited to half the ADC sample rate. Therefore, coverage of the frequency band from 800 MHz to 6 GHz, where all of today's cellular and WLAN channels lie, would require a 12 bits, 12 GS/s ADC (Bagheri et al., 2006). Figure 2.3(a) shows a rough estimation of the power needed to realize such an ADC related to a typical Figure of Merit (FoM) for ADC, defined as:

$$FoM = \frac{P_{tot}}{f_{snyq}2^{ENOB}} \tag{2.1}$$

where P_{tot} is the total power consumption, f_{snyq} is the Nyquist sampling frequency relative to the effective resolution bandwidth and $ENOB$ is the effective number of bits. This ADC is not realistic nowadays and it will

(a) Power consumption vs. FoM   (b) Year vs. FoM
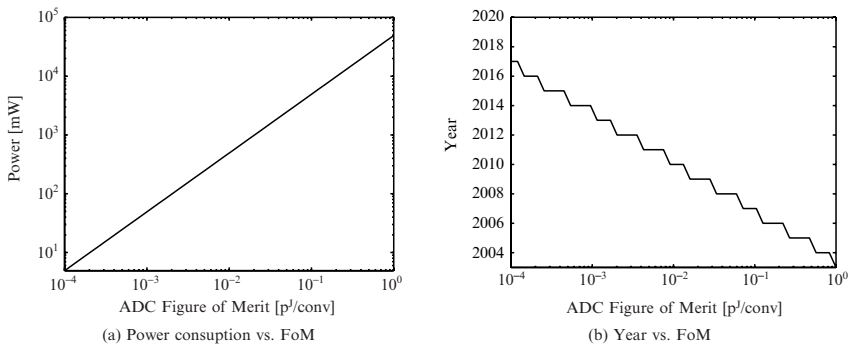
Figure 2.3.   (a) Power required to realize a 12 bit, 12 GS/s ADC and (b) foreseen improvements of the ADC FoM in the next years.

remain so in the next 10 years. Figure 2.3(b) shows indeed that if this FoM halved every year from now on, such a performing ADC could consume a reasonable amount of power only in 2016. As shown in (Walden, 1999), new challenges should be tackled to achieve this constant improvement.

- In order to allow real-time execution of software-implemented radio interface functions such as frequency conversion, digital filtering, and spreading, parallel DSPs have to be used. This also creates problems such as high circuit complexity, high power consumption, and dissipation.

Even if significant progress has been made in developing SR in the last years thanks to improvements in technologies, many issues still need a practical solution. Clearly, SR has promise, but how do we advance from current technology to the small, battery-operated device we use in the "standard" analog radios? A compromise is needed: proper partitioning of analog/digital signal processing can be a practical solution nowadays and Chapter 3 will deal with that.

2.2   Candidate Architectures for SDR Front Ends

The motivation behind the ideal SR architecture is not only the high flexibility of DSP to adapt the front end to simultaneously operate with any modulation, channel bandwidth, or carrier frequency (Abidi, 2006), but also the possible cost savings that integrating in full digital technology could yield. A full digital SR makes sense in military applications, but it far exceeds the real needs in a standard mobile handset where the need for concurrent reception is limited to a few applications. An SDR is a practical version of a SR: the received signal is sampled after a suitable analog signal processing, i.e. downconversion/ upconversion, channel selection, interference rejection, and amplification. This kind of receiver represents the likely scenario where the user selects a few channels at a time: for example, while the user is doing a phone call (GSM) by using

his wireless headset (Bluetooth), he is also downloading a file from the web (WLAN). The power consumption becomes reasonable and cost savings are still possible. However, a very flexible analog front end is required to be implemented in current IC technology. The ability to process signals corresponding to a wide range of frequency bands and channel bandwidths is a critical feature of multistandard front ends and impacts heavily the design of both analog and digital segments of the receiver.

To understand some of the barriers in different types of receiver architectures, a review is given and analyzed. This section presents a short overview of different analog front-end architectures for the implementation of multistandard SDR with respect to the current emerging technologies.

2.2.1   Heterodyne and digital-IF receivers

The heterodyne receiver translates the signal received at the antenna to a lower Intermediate Frequency (IF) by using a downconversion mixer. This operation allows to use a less-selective filter to suppress eventual interferers before the conversion to the digital domain. In this kind of receiver, because of Image Rejection and Half Intermediate Frequency issues (Razavi, 1998), it is not easy to find the best trade-off between sensitivity, normally influenced by the level of image rejection, and selectivity, defined by a channel select filter. If the IF is high, Image Rejection is easier because the needed Bandpass Filter (BPF) will require a lower quality factor, and then, its losses will also be limited. Losses reported at the first receiver stages can heavily impact the overall receiver Noise Figure (NF). On the other hand, by selecting a lower Intermediate Frequency, the channel selection filter will be less power demanding and more efficient against interferers. More than one stage of downconversion makes the trade-off easily achievable.

Figure 2.4 shows the most common heterodyne architecture in today's RF receivers: a dual IF topology exploits two downconversion stages so distributing filtering and amplification requirements on a longer chain. The first IF f_{IF1} is selected high enough to efficiently suppress the image, and the second IF f_{IF2} is selected low enough to relax the requirement on the channel selection filter. If the second IF is equal to zero, the second downconversion normally separates the signal to I (in-phase) and Q (quadrature) components for Single-Side Band (SSB) communication systems or frequency-phase-modulated signals, and the corresponding demodulation and detection are performed at baseband. This downconversion is realized by quadrature mixers, which have a $90°$ phase shift between two local oscillator signals.

However heterodyne receivers have a number of substantial problems as far as their full on-chip integration is concerned. This contrasts with the current trends in transceiver design for battery-powered devices which are pushing towards the adoption of cheap, scalable, and power-efficient radios designed
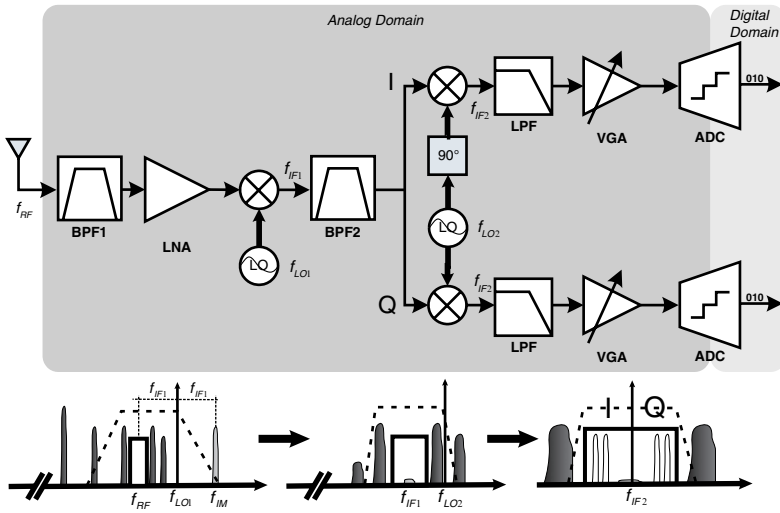
Figure 2.4.   A conventional dual-IF heterodyne architecture with quadrature downconversion at the second IF stage.
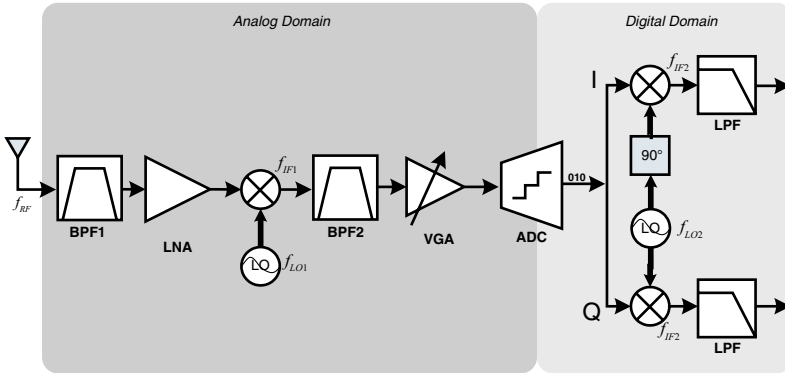
Figure 2.5.   A digital-IF heterodyne architecture with quadrature downconversion performed in the digital domain.

in digital CMOS technologies. A straightforward solution for increasing the receiver integration level is to transfer signal sampling and ADC interface from baseband to higher frequencies and to use a high-resolution ADC converter to enable further signal processing in the digital domain. A good trade-off in this sense is shown in Figure 2.5: the first IF is directly digitized; quadrature mixing and low-pass filtering are then performed in the digital domain, avoiding all the typical analog issues such as I/Q imbalance and DC offset. Although digital-IF architectures have a big potential, their main limitation is still in the performance required by the ADC, which may need sampling rates of few

hundreds Megahertz (according to the selected IF frequency), but also a very high dynamic range.

- **Advantages**

  The heterodyne receiver can easily adapt itself to many different standards requirements achieving a very good sensitivity and selectivity. DC offset of the first few stages is removed by bandpass filtering, and that of the last stage is suppressed by the total gain in the proceeding stages. As for the LO leakage, since the first mixer LO frequency is out of the band of interest, it is suppressed by the front-end bandpass filter and its radiation from the antenna is less objectionable.

- **Drawbacks**

  The need for a large number of external components, i.e. the image rejection filter, and the complexity of the structure causes problems if a high level of integration is necessary and flexibility features have to be implemented, as is the case for SDR. This is also the major drawback from the costs point of view.

2.2.2   Zero-IF receivers

The original homodyne receiver was developed in 1932 by a team of scientists searching for a method to simplify the heterodyne architecture. The new receiver was able to demodulate Amplitude Modulated (AM) signals using a local oscillator synchronized in frequency to the carrier of the wanted signal. The received signal could be direct converted to baseband, where all the unwanted interferers were rejected by an LPF. The resulting architecture had lower complexity and power consumption but suffered the high inaccuracies of discrete components. Issues like LO leakage and DC offset severely jeopardized the reception.

After the development of integrated technologies, most of those issues could be solved and, during the last decade, we have witnessed a mass migration from heterodyne to zero-IF architectures. The main reason behind this is the fact that, thanks to their simplicity, direct conversion architectures are much more suitable to monolithic integration than heterodyne and definitely cheaper (Abidi, 1995). The modern zero-IF receiver is no longer limited to the reception of AM signals, now being able to process more complex modulation schemes such as frequency and phase modulations by means of quadrature downconversion. A typical direct conversion receiver is shown in Figure 2.6. The RF band is selected by an external passive filter and the signal is amplified by an LNA, as in the superheterodyne architecture. The signal is then mixed directly to DC by a RF quadrature mixer, hence, the rest of the passive filters and mixing stages are unnecessary. Compared to Figure 2.4, it is evident the reduced number of analog components. Though, many of these components are much
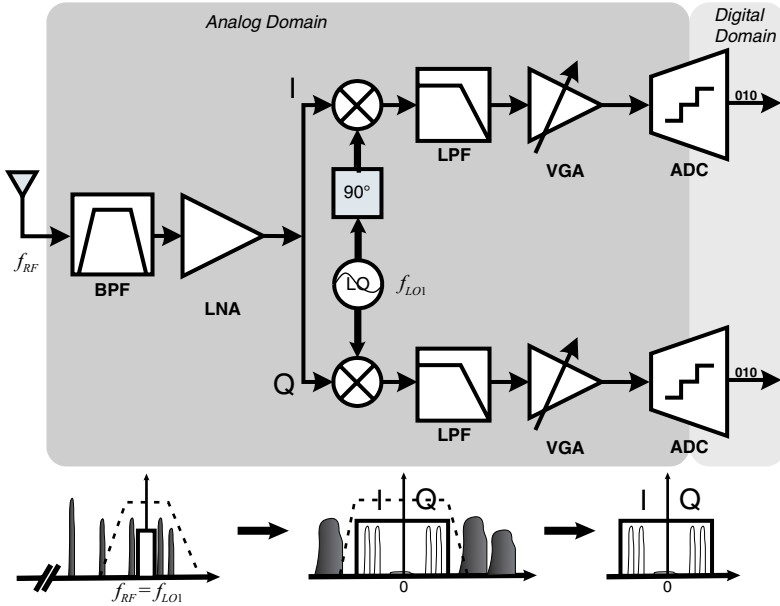
Figure 2.6.   Direct conversion (zero-IF) receiver architecture.

more difficult to design: i.e. the channel select filter, which is responsible for rejection of interferers and anti-aliasing, presents severe power-linearity-noise trade-offs. An accurate gain distribution at baseband may often mitigate this severe specifications.

The direct translation to DC can though, generate issues that are of minor importance in heterodyne receivers. *DC offset* (Svitek and Raman, 2005) can be generated due to LO leakage and components mismatches. If large enough, it might swamp the baseband amplifiers and destroy signal reception. *Flicker noise*, normally negligible in heterodyne receivers, may have here a significant impact on the overall receiver NF, mostly for low bandwidth standards such as GSM. Another major problem of direct conversion receivers can be *second-order intermodulation*. In frequency division duplexing access techniques, the transmitter leakage into the receiver produces second-order intermodulation products around DC. In presence of minimum received signals these can easily limit the achievable signal to noise plus interference ratio. For example, in UMTS terrestrial radio access – frequency division duplexing system, Input Intercept Second-Order Power (IIP2) values at receiver input as high as about 48 dBm are required (Mastretta and Svelto, 2002). Finally, the I and Q channels of a zero-IF receiver carry orthogonal channels of information. However, mismatch in the gain or phase between the two channels results in interference, which makes it more difficult to recover the information they contain as it results
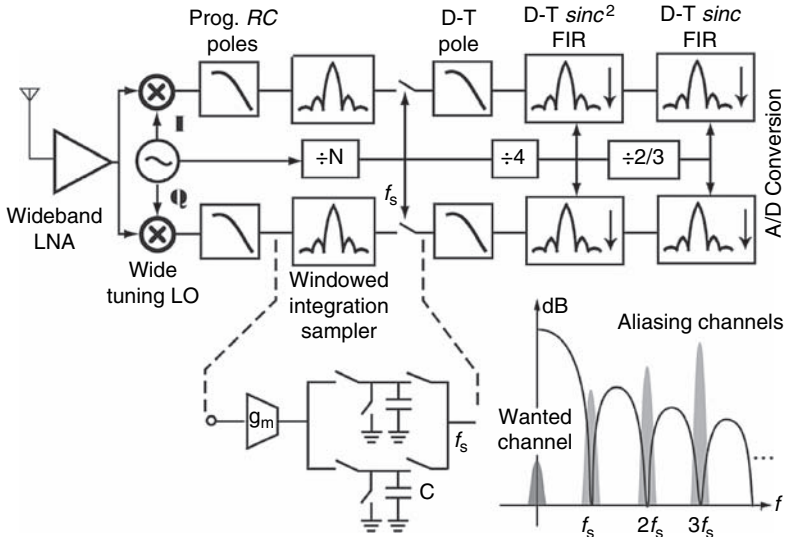
Figure 2.7. An example of SDR receiver based on a discrete-time zero-IF architecture presented by UCLA in Abidi (2007).

in a corruption of the Bit Error Rate (BER) and therefore the signal constellation. Modern digital communication systems specify a maximum Error Vector Magnitude (EVM), typically on the order of a few percent, which can be related to the *gain and phase mismatch error of the I/Q channels*.

As far as flexibility in a zero-IF receiver is concerned, its relative simplicity and minimum components count made it one of the most popular architecture for multistandard receivers (Woonyun et al., 2005, 2006). An attempt to implement a SDR front end based on a *Discrete-Time zero-IF* architecture was presented in (Abidi, 2007). As shown in Figure 2.7, the receiver comprises an LNA spanning a pass-band from 800 MHz to 6 GHz (Chehrazi et al., 2005), and a wideband LO generator that tunes to important bands in this range based on two tunable Voltage-Controlled Oscillator (VCO)s. The authors claim there is no need for a RF preselect filter before or after the LNA. Though this choice moves down to the mixer very tough linearity specifications. Ones at baseband, a discrete-time signal processing is enabled by a windowed integration sampler (Yuan, 2000). The circuit, implemented with a switched capacitors/transconductors technique, filters its continuous-time input by a *sinc* function prior to sampling, with nulls in its transfer function at all multiples of the sample frequency and it is preceded by two passive programmable real poles to achieve enough selectivity (Bagheri et al., 2006). Before the Analog to Digital conversion, the sampling rate is decimated with anti-aliasing passive switched-capacitor FIR filters.

- **Advantages**

  Zero-IF architectures guarantee a high level of integration thanks to their simplicity. They do not require any high-frequency bandpass filter between LNA and mixer, which is usually implemented off-chip in a heterodyne receiver for appropriate selectivity. Direct conversion receivers do not suffer the image problem as the incoming RF signal is downconverted directly to baseband without any IF stage.

- **Drawbacks**

  An RF prefilter is always needed before the LNA to attenuate large blockers. This may limit the transceiver flexibility. Severe DC offset can be generated at the output of the mixer when the leakage from the LO is mixed with the LO signal itself. This could saturate the following stages and affect the signal detection process leading to I/Q mismatch and even-order distortion. Also, since the mixer output is a baseband signal, it can easily be corrupted by the large flicker noise of the mixer, especially when the incoming RF signal is weak.

2.2.3 Digital low-IF receivers

The low IF receiver architecture combines the advantages (and drawbacks) of heterodyne receivers and direct conversion receivers. As illustrated in Figure 2.8, the RF signal is mixed down to a nonzero low or moderate IF, normally centered around a few hundred kilohertz up to several megahertz (normally 1/2, 1,
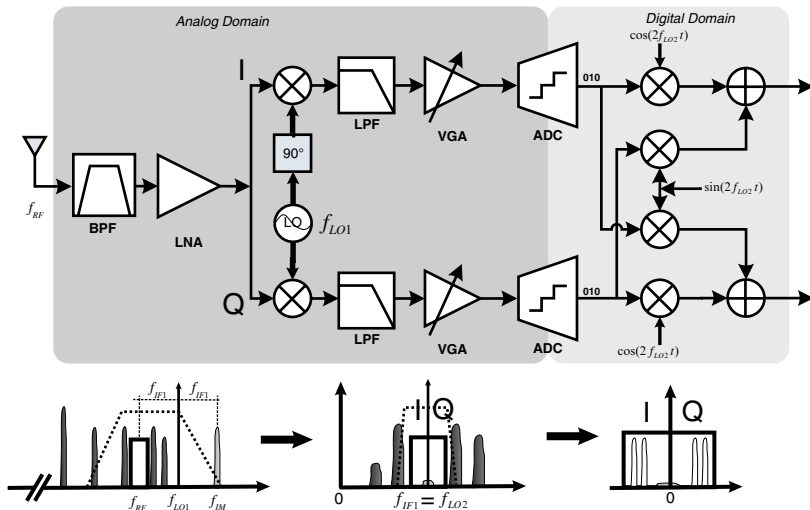

Figure 2.8. Digital low-IF receiver architecture.

or 2 channel bandwidths). The channel select filter must be a complex Band-pass Filter (BPF). Following amplification, the signal is then converted to the digital domain with an ADC. The final stage of downconversion to baseband is then performed digitally with channel filtering implemented through DSP techniques.

As the image frequency problem is reintroduced in this kind of receivers, it has to be taken into account in the receiver planning. Image signal and unwanted blockers are normally rejected by quadrature downconversion (complex mixing) and subsequent polyphase filtering. The best IF selection results in the best trade-off between the requirements for the polyphase filter and the ADC. After A/D conversion the signal is digitally downconverted to baseband before digital filtering. A digital mixer can then be used for the final downconversion to baseband where digital channel filtering is performed. The migration of these traditionally analog functions into the digital domain offers significant advantages. The digital signal processing is immune to operating condition variations that would corrupt sensitive analog circuits. Using digital signal processing improves design flexibility and leverages the high integration potential, scalability, and low-cost structure of CMOS process technologies. While the digital low-IF receiver does add a downconversion stage, because the extra stage is digital, it is possible to implement this functionality in an area smaller than that occupied by the analog baseband filter of the zero-IF architecture. In addition to that, since the desired signal is 100 kHz above the baseband after the first analog downconversion, any DC offsets are of negligible concern. Also once in the digital domain, digital filtering is successful in removing any potential issue. The immunity to DC offset has the benefit of expanding part selection and improving manufacturing. At the front end, input SAW filters requirements are relaxed w.r.t. heterodyne solutions, and the board design is simplified.

An example of this architecture for a dual-standard receiver was presented in (Yoshida et al., 2000) by Toshiba. Two critical points could be detected here: a flexible antenna RF prefilter is still needed to bandlimit the receiver input and the ADC requires relatively tough performances (12 bits, 64 MHz). In addition to that, gain mismatch in the I/Q ADCs worsens image rejection.

- **Advantages**
  The low-IF architecture still allows a high level of integration (no need for off-chip IF SAW). In addition to that, since the wanted signal is not situated around DC, issues like DC offset, flicker noise and LO self mixing can be easily avoided. the digital baseband processing allows integration potential, scalability, and low costs.

- **Drawbacks**
  Low-IF receivers may require large Image Rejection Ratio (IRR). However an appropriate level of image rejection can still be achieved with a

well-designed quadrature downconverter and integrated I and Q signal paths. I/Q imbalances cause interference that cannot be removed in later stages and so directly decrease the image-reject capabilities of the front end.

2.2.4   Bandpass sampling receivers

Bandpass sampling can be an alternative solution to relocate a signal with limited bandwidth $B = f_H - f_L$ from an RF frequency f_{RF} down to baseband. This occurs because sampling in time domain is a multiplication of the signal by a comb of unitary pulses, which in frequency domain becomes a convolution of the Fourier-transformed unitary pulses with the spectrum of the signal. The various spectrum replicas do not overlap one another only if subsampling is performed at the correct frequency. According to the Shannon's sampling theorem, a signal $s(t)$ of bandwidth B can be reconstructed from samples $s(n)$ taken at the Nyquist rate $2B$ samples per second using the interpolation formula:

$$\hat{s}(t) = \sum_n s\left(\frac{n}{2B}\right) \frac{sin[2\pi B(t - n/2B)]}{2\pi B(t - n/2B)} \tag{2.2}$$

According to the position of the signal bandwidth, different situations can be depicted. Figure 2.9 shows the classical bandpass theorem for Uniform Bandpass Sampling (UBPS) which states that the signal can be reconstructed
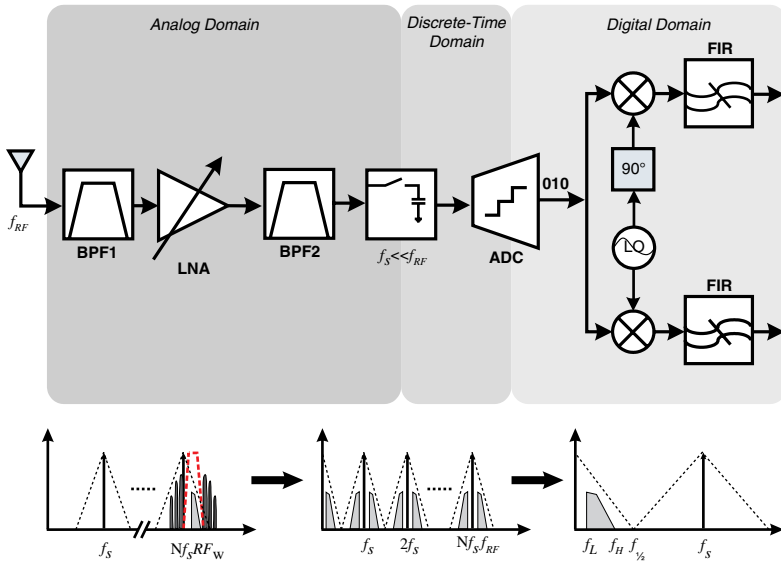

Figure 2.9.   Uniform bandpass sampling receiver.

if the sampling rate is at least $f_s = 2B$. After sampling, the folded spectrum has an unambiguous range of $[0, f_s/2]$. In addition to the fact that this is only applicable for integer band positioning (Vaughan et al., 1991), this theoretical minimum sampling rate makes the system very sensitive to any imperfection of the transceiver, easily yielding to disruptive aliasing. Therefore the choice of the sampling frequency is critical in this configuration. As for any sampled data system, a bandpass sampling receiver must be preceded by a very selective bandpass filter to remove possible interferers that otherwise would be aliased to baseband. The noise left out is folded at baseband together with the signal yielding to a degradation of the Signal to Noise Ratio (SNR) given by:

$$SNR = 10log_{10}\left(\frac{S}{N_p + (n-1)N_o}\right) \tag{2.3}$$

where N_p and N_o are the in-band and out of band noise and n is the number of aliasing Nyquist regions. Even if the sampling frequency is much lower than the RF frequency, the performance required for the sampler and ADC may require a high power consumption.

A flexible transceiver of this kind was presented in (Akos et al., 1999). This front end requires a prefilter before the LNA to attenuate wide-band LNA noise that would otherwise accumulate after sampling. A sampling rate of 24.2 MHz positions the two bands side-by-side in the effective IF range from DC to 12 MHz. This example is interesting because it illustrates how a single sampling action effects two different frequency translations. However, again, the need for RF prefilters limits the receiver's flexibility.

If the RF signal is split into two paths and each part is uniformly sampled at f_s leading to an unambiguous range at baseband of $[-f_s/2, f_s/2]$, we are doing Quadrature Bandpass Sampling (QBPS). QBPS not only provides the quadrature components, but also significantly relaxes the choice of the f_s. As shown in Figure 2.10, such receiver requires an analog RF signal conditioning before the ADC that should perform downconversion, filtering, and sampling. This allows to have high-speed discrete-time Analog to Digital conversion at IF with reduced resolution. A subsampling mixer can perform the tasks of signal downconversion and sample-and-hold operation simultaneously. However, simple subsampling downconverters lack the filtering properties required to suppress unwanted interfering signals and wide-band noise aliasing on top of the wanted signal in the subsampling process. On the other hand, integration of a steep continuous-time bandpass anti-aliasing filter in front of the sampler is difficult at high frequencies.

A receiver architecture based on RF sampling downconversion filter was proposed in (Jakonis et al., 2005). This discrete time block combines RF sampling and quadrature downconversion with tunable anti-aliasing filtering at intermediate frequency and decimation of the sampling rate. For a proper choice of
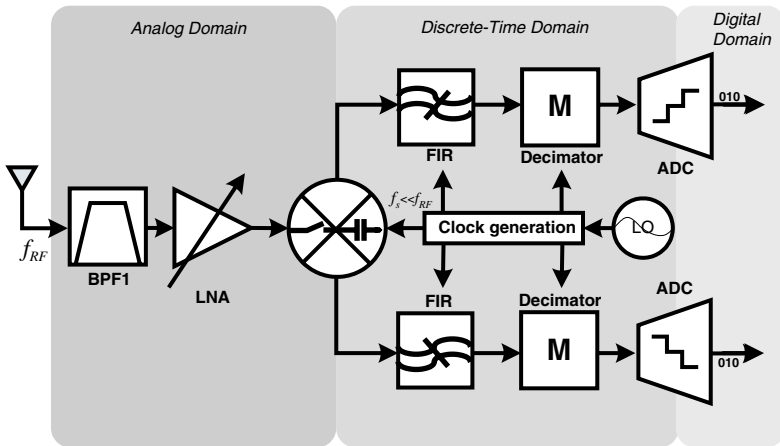
Figure 2.10.   Quadrature bandpass sampling receiver.

sampling rate in the sampling Mixer, I/Q components are obtained using a single-phase Local Oscillator (LO). However, noise aliasing into the baseband is till an issue, I/Q imbalance degrades the image rejection and the receiver is sensitive to the clock jitter. The realization of a narrow-band channel selection filter operating at a high sampling frequency in order to attenuate strong interferers can be difficult with conventional switched-capacitor (SC) filter design techniques. A technique to overcome this issue is proposed in Karvonen et al. (2005, 2006): this approach combines Finite-Impulse Response (FIR) anti-aliasing and image rejection filtering, quadrature downconversion by subsampling and Infinite-Impulse Response (IIR) channel selection filtering into one functional sampler block. The frequency $1/4T$ of mixer switching is linked by a simple counter to the output sample rate $1/NT$, where N is programmable. This might be an issue at very high operation frequencies.

- **Advantages**
  The inherent demodulation of the input makes subsampling attractive for communication systems as no mixer is needed for downconversion. The architecture is relatively simple, and standard receivers issues such as I/Q and DC offset are avoided.

- **Drawbacks**
  Bandpass sampling requires very tough RF BPF specifications. The SNR is not preserved due to the noise aliasing. Clock jitter can be critical.

2.2.5   Direct RF sampling receivers

Recent advances in IC technologies made it possible to explore more extreme approaches like direct RF sampling techniques: in this kind of receivers, the
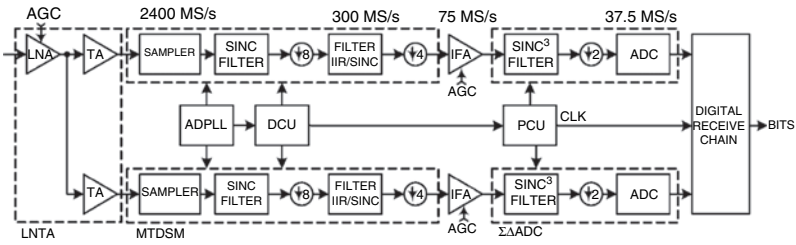
Figure 2.11. Bluetooth receiver from Texas Instruments exploits a direct RF sampling architecture. (From Staszewski et al., 2004.)

front end uses no analog frequency down conversion. Discrete-time analog signal processing is indeed used to sample the RF signal as it is downconverted, downsampled, filtered, and converted to the digital domain. This approach helps to relieve the analog design complexity and it might allow reduction of costs and power consumption as required in a reconfigurable design environment. While in bandpass sampling receivers operate at lower IF but suffer from noise folding and clock jitter, direct RF sampling avoids those effects and achieves great selectivity at the mixer level. The selectivity is normally controlled by the LO clock frequency, which are extremely accurate in deep submicron CMOS processes.

Texas Instruments recently implemented two digital CMOS transceiver of this kind (Staszewski et al., 2004; Muhammad et al., 2006) aiming at moving to the digital domain most of the signal processing operations normally performed in the analog domain. The main philosophy behind this approach is to provide all the filtering required by the standard as early as possible in the receiving chain so relaxing the design requirements for the baseband amplifiers. The block diagram of this receiver is shown in Figure 2.11, for both analog and digital parts. The analog front end includes simply a low-noise transconductance amplifier (LNTA): its output current is integrated on a switched capacitor array at the LO frequency (2.4 GS/s). A series of decimation and filtering functions follow the RF sampling before the analog to digital conversion, performed by a Sigma–Delta ADC.

Even if the TI implementations are not SDR, as the circuits are tuned respectively for Bluetooth and GSM, the approach has definitely big potential and could be further exploited in the flexibility perspective.

2.3   SDR Front End Implementation

A well-designed architecture of a multistandard receiver should optimally share the available hardware resources and make use of tunable and software programmable devices. From the viewpoint of reconfigurable radios, the zero-IF receiver is the best candidate to realize such SDR as it has the highest potential

to reduce cost, size and power, even under flexibility constraints. This is why this architecture will be our reference for the rest of this book.

A fully reconfigurable zero-IF SDR front end is proposed here (Craninckx et al., 2007; Ingels et al., 2007) that exploits extensive migration towards digitally assisted analog blocks. The primary idea behind this is the addition of numerous configuration *knobs* to a classical front end, such that its performance can be tuned to any of all the specific requirements of the envisioned standards to be covered. These should not only cover a limited set of operation modes as in e.g. (Abidi, 2007). From the viewpoint of functionality, the RF carrier frequency, the channel bandwidth, the noise figure, the linearity, the filter characteristic, etc. should all be reconfigurable over a very wide range. But there is also an equally important viewpoint of *energy optimization*, which allows the front end to use the same reconfiguration knobs to reduce its power consumption in a particular mode when allowed by the conditions of the environment, e.g. reduce the filtering level when the interferer level is lower than the worst case defined by the standard. This enables the SDR front end to fulfill the specifications of each standard (at a power similar to a single-mode radio) but still operate at significantly lower average power consumption due to real-time power/performance trade-offs.

A conceptual view on the physical implementation of this SDR transceiver front end is shown in Figure 2.12. The core of the transceiver is of course the silicon active IC, implemented in a plain CMOS technology. Because of the high volumes and the associated requirement for low cost these energy-efficient
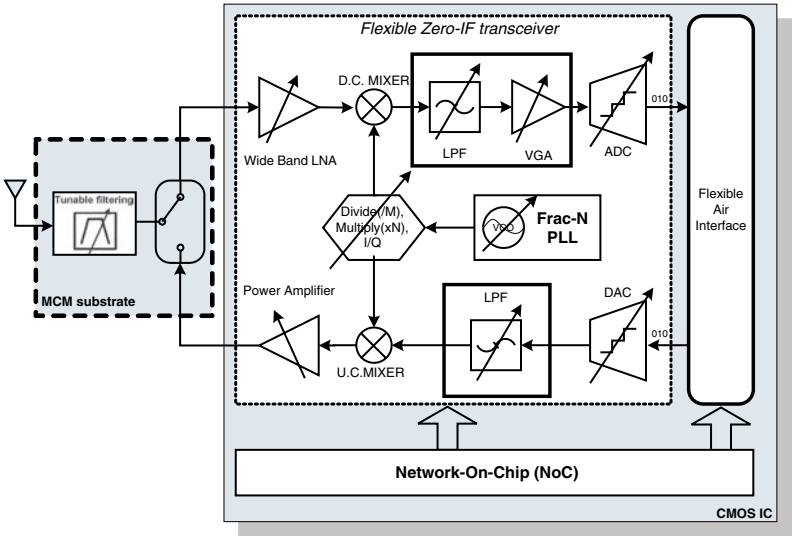

Figure 2.12.   Simplified block diagram of the zero-IF SDR transceiver implemented in IMEC.

multimode radios must obtain, and the possible implementation together with the digital processor on a single die, the use of plain CMOS is a must. A 0.13 μm node is used here because of its relatively cheap availability, but commercial implementations should be able to use the scaling benefits of lower technology nodes. The silicon IC actually implements a fully reconfigurable direct conversion receiver, transmitter, and two frequency synthesizers. Direct conversion is the only architecture able to be reconfigured over such a broad range, it would be impossible to find, for example a common IF suitable for all standards in a heterodyne architecture. A key aspect of a multimode operation is its interference robustness, which necessitates the use of tunable narrow-band circuits at the antenna interface. Indeed, wideband circuits without filtering at the RF in and output will never be able to withstand the blocking requirements needed for simultaneous multimode operation.

2.3.1 LNA and input matching

In this receiver, the option of using MEMS switches to build a low-loss reconfigurable antenna filter section on a thin-film substrate is explored. This is particularly the case for the LNA, of which the active CMOS part has been co-designed with the MEMS switch and the passive off-chip matching (Liu et al., 2007). The circuit schematic of Figure 2.13 shows that multiband operation has been achieved without touching the inductive emitter degeneration. An SPDT MEMS switch is used to connect the LNA to either its 1.8 GHz matching
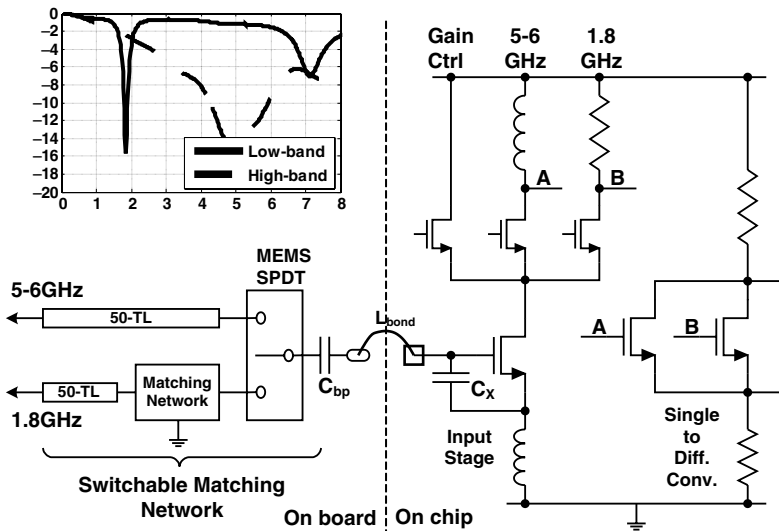

Figure 2.13. IMEC SDR front end: CMOS/MEMS co-designed dual-band LNA circuit schematic and input matching measurement.

circuit and antenna filter, or to its 5 GHz section which uses just the bonding wire for input matching. Because the thin-film MEMS technology was not mature enough, a commercial MEMS switch was mounted on a Printed Circuit Board (PCB) together with the CMOS die, which has of course limited the amount of reconfigurability of the circuit. Nevertheless, the loss of the switch including its package was measured to be only 0.2 dB. When a mature technology that integrates MEMS switches in an MCM-D technology becomes available, more complex structures will become feasible and the high-frequency performance will even improve because of the absence of the package around each switch. Internally, the LNA has an LC-tuned output branch for the high band, and a resistively loaded branch for frequencies lower than 2.5 GHz. A shunt cascade branch is provided for gain switching. Both outputs pass through a multiplexing single-to-differential converter towards the direct downconversion mixer, which has a current-mode output with a 7-bit programmable gain.

2.3.2   Frequency synthesizer

The frequency synthesizer block diagram is shown in Figure 2.14. Two of them are integrated on chip for FDD frequency synthesis. Each contains a wide-tuning range VCO with switchable active core and sensitivity (Hauspie et al., 2006), as well as a programmable charge pump and loop filter. A fully flexible VCO distribution network routes the 3–5 GHz signal of each Phase-Locked Loop (PLL) (or of an external source) to the receiver, the transmitter, and/or
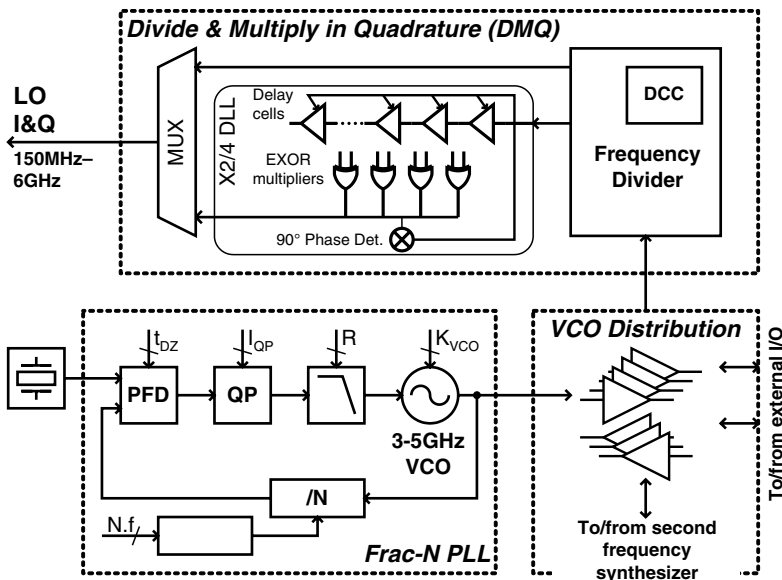

Figure 2.14.   IMEC SDR front end: multiple-decade frequency synthesizer block diagram.

the external world. This external interface is required for MIMO operation, where multiple transceiver ICs need to share a common LO signal, generated by one of them. Then the actual LO generation happens in the Divide-Multiply-Quadrature (DMQ) block placed just before the mixers. This circuit generates quadrature LO signals in the whole band from 6 GHz down to 150 MHz, with the constraint that the VCO never runs at the RF frequency to avoid the well-known direct conversion problem. The most obvious block used for this is frequency division by a programmable modulus ranging from 2 to 20. Since division by an odd number cannot generate quadrature signals, a Duty Cycle Correction (DCC) block is foreseen. Quadrature LO signals higher than 2.5 GHz cannot be generated by simple division, in this case the divider output is multiplied again by means of a 90º DLL to provide signals up to 6 GHz. For transmission, a direct upconversion architecture uses a similar reconfigurable low-pass filter, Gilbert mixers and a wideband output driver.

2.3.3 Baseband signal processing

RX channel filtering is provided by a cascade of Active-g_m-RC biquadratic cells that can independently set its order and R and C values, and therefore provides a channel bandwidth continuously programmable between 350 kHz and 23 MHz, second-, fourth-, or sixth-order transfer function, and an input referred noise level perfectly proportional to the power consumption (Giannini et al., 2006b). Also the variable gain amplifier can program not only its gain in 3 dB steps, but also its bandwidth and noise level. This baseband section will be described in detail in Section 5.3.1.

2.3.4 Measurements results

Since an enormous amount of bits are used to control the settings of each building block, a scalable NoC was integrated that is able to control each circuit based on the input data it gets from a serial interface. Figure 2.15 shows the photo of the IC ($3.0 \cdot 3.8$ mm^2) and its implementation on PCB together with the MEMS switch. A receive budget measurement is shown in Figure 2.16 for three different channel bandwidths indicating of course the Signal to Noise and Distortion ratio (SNAD) is limited by thermal noise for low input powers (total NF = 6 dB including PCB) and distortion at high input powers (IIP3 = -10 dBm). Depending on the specific system requirements in each mode, all building blocks are appropriately controlled through the NoC and performance can be varied widely. Only a few extreme cases are listed, but all intermediate settings are also available. The very wide reconfiguration range achieved without compromising actual performance shows that this prototype has taken an important step towards a true energy-efficient multimode SDR.
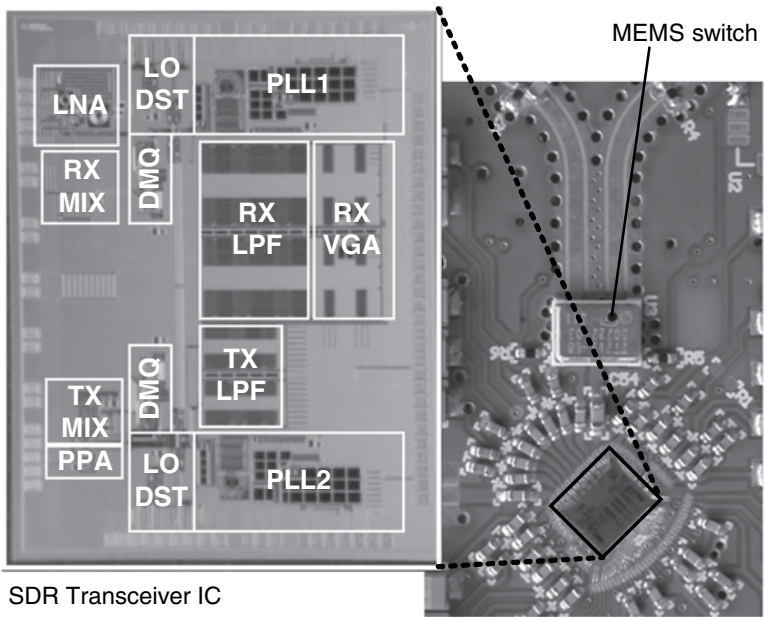
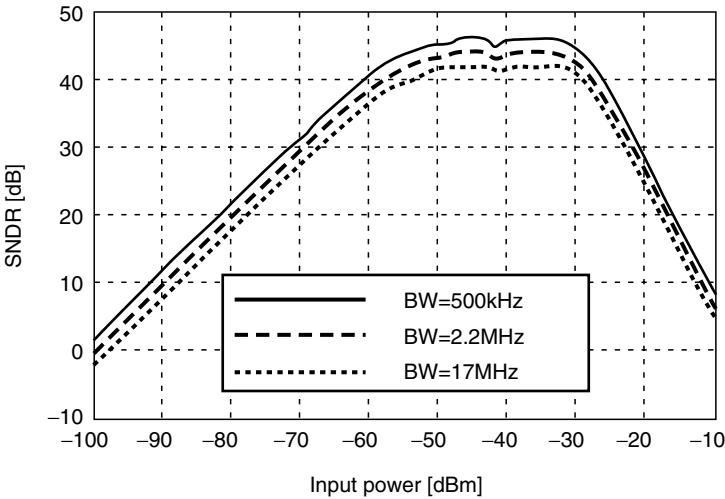*Figure 2.15.*   IMEC SDR front end: Die photo and MEMS PCB.

Figure 2.16.   IMEC SDR front end: RX measurements.

2.4   Digital Calibration of Analog Imperfections

In a multimode zero-IF transceiver, design specifications normally span over a broad range of present and future standards. Evidently, this overloads the design requirements and hampers effective design. An alternative is to design according to realistic design requirements and to digitally calibrate the front end for its eventual imperfections. The goal of calibration is to improve or optimize the performance of a full IC transceiver. In this sense, calibration relaxes the design requirements for multimode systems and enables the use of a low-cost architecture while being compliant with a broad range of standards. In the context of multimode systems, calibration should be dynamic, efficient, automatic, and implemented in the system. Calibration consists typically of two steps:

- **Characterization**
  The system imperfections are estimated. Characterization should be performed at discrete-time instances, namely at system start-up, at mode handover and/or at system defined time instances while the compensation is continuously active and updated by the characterization results. Given the discrete nature of the characterization, most of today's calibration techniques are required to deactivate system's normal operation which is hardly favorable. Moreover, the characterization accuracy will be hampered as the calibration is performed under abnormal operation conditions. Fortunately, some alternative techniques exist allowing the system to remain operational during calibration. When considering multimode MIMO systems, seamless mode handover can be established by gradually reconfiguring and calibrating the different transceivers between the different modes. In this way, the system remains operational and standard compliant during mode handover.

- **Compensation**
  Once the imperfections of the receiver are characterized, the obtained information is used to optimize its performance. This optimization is achieved by digital pre- and post-compensation of the baseband time-domain signal. Applying this compensation in the digital domain enables stable and easy implementation without the need for additional analog circuitry whereas applying it in the time domain enables compensation of any data stream, independent of its mode or modulation scheme thus ideally suited for multimode systems.

Calibration is one of the keys to enable the realization of low-cost, high-performance SDR mobile terminal. However, the cost required can be sometimes high: calibration often requires additional circuitry and thus increases the design complexity and cost. Fully analog high-frequency calibration techniques are therefore rejected as potential candidates. The only relevant techniques in

the SDR context are the digital calibration techniques which will be briefly discussed in this section for each relevant analog imperfections in zero-IF architectures.

2.4.1 Quadrature imbalance

In homodyne receiver, the RF signal is directly downconverted to a complex-valued baseband signal. The complex-valued baseband signals consists of a real (I) and an imaginary (Q) part and the LO signal consists of two signals at the carrier frequency shifted in phase by $90°$. In practical implementation, slight mismatches between the I and Q path and imperfect $90°$ phase shift between the LO paths result in a quadrature imbalance for both transmitter and receiver chain. The quadrature imbalance is generally characterized by its amplitude mismatch ε and its phase mismatch $\Delta\phi$, but for calculations, the complex-valued parameters α and β are normally used. When providing a time-domain signal $\underline{x}$ to such quadrature imbalance, the resulting signal will be (Bougard et al., 2006):

$$\underline{y} = \alpha \cdot \underline{x} + \beta \cdot \underline{x}^* \tag{2.4}$$

where $()^*$ stands for the complex conjugate. This will result in

$$\begin{cases} \alpha = cos(\Delta\phi) + j \cdot \varepsilon \cdot sin(\Delta\phi) \\ \beta = \varepsilon \cdot cos(\Delta\phi) - j \cdot sin(\Delta\phi) \end{cases} \tag{2.5}$$

Equation 2.4 can be easily transformed to the frequency domain such that:

$$\underline{Y} = \alpha \cdot \underline{X} + \beta \cdot \underline{X}_m^* \tag{2.6}$$

where $()_m$ denotes the mirroring or imaging operation in which the vector indices are mirrored to DC such that:

$$\overline{k'} = |\overline{k_{tot}} - \overline{k} + 1, \overline{k_{tot}}| + 1 \tag{2.7}$$

where $\overline{k'}$ denotes the total amount of indices of the mirrored vector index of $\overline{k}$ and $\overline{k_{tot}}$. Quadrature imbalance thus modifies the spectral content of $\underline{x}$ and causes spectral components at the image frequencies (mirrored indices) of its data carriers. As in multicarrier modulation the data carriers are generally symmetrically spaced, quadrature imbalance will directly degrade the quality of each of the data carriers and hence degrade system performance. The impact of the quadrature imbalance is generally quantified as Negative Frequency Rejection (NFR), indicating the power difference between the wanted spectral components and its image:

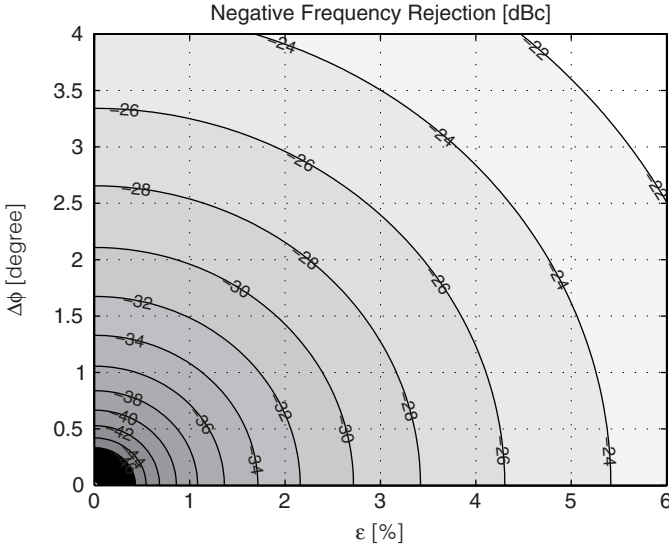$$NFR = 10log_{10}(\varepsilon^2 + tan^2(\Delta\phi)) \tag{2.8}$$

Figure 2.17. Quadrature imbalance related to negative frequency rejection.

The relation between the quadrature imbalance and the NFR is illustrated in Figure 2.17.

Different quadrature imbalance characterization techniques exist at the receiver side, mainly based on adaptive filtering (Schuchert et al., 2001; Valkama et al., 2001). As these techniques exhibit slow convergence, they are applicable in steaming modes only. An alternative technique is presented in (Tubbax et al., 2003), where quadrature imbalance characterization is performed based on one calibration measurement. This fast convergence builds on the realistic assumption of a smooth channel between the transmitter and receiver system. The main drawback of all mentioned receiver characterization techniques is however the need for a quadrature imbalance-free generated transmitter signal and thus an ideal transmitter. A promising technique is presented in (Debaillie, 2007), where the quadrature imbalance of the transmitter and receiver system is characterized separately based on a single calibration measurement. This technique might be perfectly suited in the multimode context. Realistic values of transmitter and receiver quadrature imbalance range up to 5%, 6° and -20 dBc for ε, $\Delta\phi$, and NFR, respectively. After calibration, the remaining transmitter and receiver quadrature imbalance should be lower than -35 dBc.

Pre- and post-compensation enhances the signal quality by manipulating its baseband signal inversely to its imperfection. In terms of carrier feedthrough, this inverse operation is simple: subtraction of the complex DC offset estimated during characterization from the digital baseband signal will generate a spectral
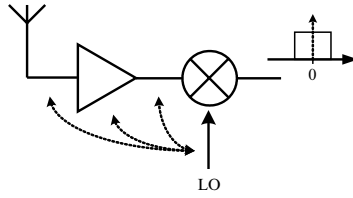
Figure 2.18.   Parasitic coupling between the LO path and the RF path causes self-mixing and creation of a DC offset on the baseband signal.

carrier at the transmitter output that is opposite to the tone caused by carrier feedthrough. In terms of quadrature imbalance, this results in:

$$\underline{y} = \frac{\alpha^* \cdot \underline{x} - \beta \cdot \underline{x}^*}{|\alpha|^2 - |\beta|^2} \tag{2.9}$$

where $\underline{y}$ represents the pre-compensated time-domain signal applied to the analog transmitter or the post-compensated time-domain signal applied to the digital receiver and $\underline{x}$ represents the time-domain signal coming from the digital transmitter or the time-domain signal coming from to the analog receiver.

2.4.2   DC offset

In direct conversion receivers, parasitic coupling between the LO path and the RF path in both directions will cause self-mixing and creation of a DC offset at the baseband signal (Razavi, 1998) as shown in Figure 2.18. This DC offset decreases the effective dynamic signal swing, especially when the received signal power is low, and therefore reduces the gain and linearity performances of the receiver. Using a high-pass filter to remove the DC offset from the base band signal is not an option: the targeted standards have a dense spectral occupation and such filters cannot be implemented efficiently. Therefore, another calibration technique should be used.

As the DC offset in the receiver path is mainly generated in the mixer, to limit its impact it should also be removed as close as possible to this mixer in the baseband path. Haspeslagh et al. (1992) suggest an architecture adding a digitally controlled complex compensation DC offset directly after the mixer. Building on similar architectural approach (Come et al., 2004; Debaillie, 2007) present characterization algorithms that find the optimal complex compensation DC value while keeping the system operational. Both techniques provide very fast convergence and are thus applicable in the multimode transceivers.

2.4.3   Impact of LPF spectral behavior

When designing filters either analog or digital in the signal path, their spectral behavior is not the only concern. As further discussed in Section 3.9,

in multicarrier modes applying Orthogonal Frequency-Division Multiplexing (OFDM) schemes, the system performance may degrade drastically due to the extension of the impulse response between the digital transmitter and receiver. As demodulation in an OFDM receiver is based on frequency-domain block processing, the accumulation of the signal path filters and the multipath channel might cause Inter-Symbol Interference (ISI) and Inter Carrier Interference (ICI). This interference is generally prevented by inserting a Cyclic Prefix (CP) with a minimal length equal to the significant part of the equivalent baseband channel impulse response. The response of the channel in an indoor WLAN system is typically short (<500 ns in IEEE802.11a) but in combination with the transmit/receive filters, the length of the total impulse response is likely to exceed the cyclic prefix. This effect can be reduced by appropriate time synchronization at the receiver, as described in Muller-Weinfurtner (1999) and Pollet and Peeters (1999) where the optimal synchronization minimizing the ISI and ICI is explained. A simulation tool has been described in Debaillie et al. (2001) that efficiently analyzes the impact of a filter chain on the amount of ISI and ICI injected in the system and thus enables filter architecture selection and filter design while minimizing the system performance degradation.

In contrast to the other characterizations, the spectral behavior calibration of the LPF can be performed completely at baseband; few baseband switches connect (part of) the analog baseband circuitry in-between the transceiver's baseband input and output. In given configuration, the spectral behavior or transfer function can be characterized by comparing the digital signal before and after propagation through the analog circuit. When using a multitone signal with a relative dense and sufficiently wide spectral content, the cut-off frequency, the in-band ripple, and the spectral phase relation can be easily characterized.

2.5   Conclusions

In this chapter, we reviewed the main issues related with the design of RF front end for a SDR flexible transceiver capable of accommodating most of the present mobile standards. SDR RF hardware design has significant differences compared to "traditional" single-mode requirements as the operating frequency, the channel bandwidth and the channel conditions (interferers, etc.) are variable. These factors give rise to major design challenges with transceiver filtering and linearity. These factors will provide RF engineers with significant challenges over the next years. Based on the discussions and arguments of this chapter on different possible architectures, we can draw the following conclusions:

- A flexible radio capable of accommodating today's major standards represents a major first step on the SDR path. While there is a possibility that the RF front-end technology will advance sufficiently near-term to get rid of the multiple RF chains, some promising analog techniques are being exercised

to reduce their impact on size, power, and cost of a fully integrated SDR terminal.

- In all the architecture presented, design challenges are present in the design of a flexible RF prefilter. New technology solutions are here needed that go beyond the analog/digital word following the more than Moore path where MEMS technology will have a major role.

- From the SDR perspective, the zero-IF architecture seems to be the most promising approach. The conventional imperfections of this architecture can be easily compensated in the the digital domain. However, flexibility, imposes tough challenges for the design of "clean" analog circuits for both RF and baseband sections: wideband/flexible LNAs, power amplifiers, mixers, local oscillators, as well as filters and analog to digital converters are needed to build a polyvalent analog transceiver.

LINK BUDGET ANALYSIS IN THE SDR ANALOG BASEBAND SECTION

Iɴ a direct conversion receiver, the analog baseband section is responsible for adjacent channel selectivity, anti-aliasing filtering and dynamic range maximization. In the context of SDR, the analog circuits part of it are subjected to variable specifications: their requirements include the dynamic range and the Signal to Noise Ratio for the ADC and Automatic Gain Control, selectivity, noise, and linearity for the channel-select filter. This chapter discusses these specifications for a multimode reconfigurable SDR front end. The reference radio architecture is a flexible zero-IF transceiver (Section 2.3). A discussion is carried on the optimal specifications aiming at the receiver power minimization.

3.1 Analog Baseband Signal Processing

As discussed in Section 2.1, an ADC at the antenna which digitizes different wireless bandwidths simultaneously is not realizable in the foreseeable future. A practical SDR receiver will need a wide-band RF front end that can be tuned to any carrier frequency and channel bandwidth at a time: the Zero-IF architecture is the most attractive solution to achieve this goal thanks to its relative simplicity which means less complexity for a wanted level of flexibility. The analog signal conditioning at baseband normally involves filtering and amplification operations that allow the conversion to the digital domain to be efficiently performed. Figure 3.1 shows a block scheme of the baseband section intended
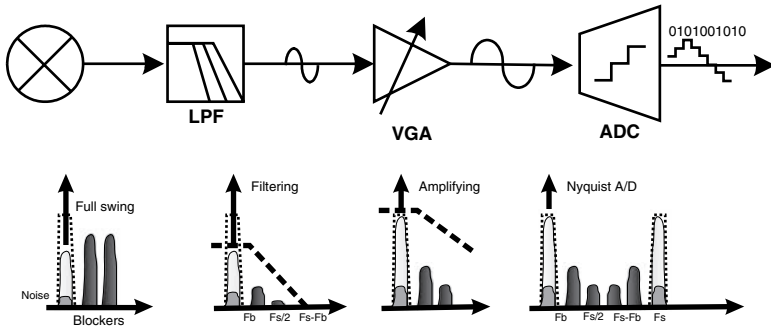
Figure 3.1.   Zero-IF baseband section operation. Filtering, amplifying and analog to digital conversion are shown.

for a Zero-IF receiver. Let us summarize the role of each analog baseband circuit for a direct conversion receiver:

- The Low-Pass Filter has mainly an anti-aliasing function, i.e. it should limit the signal bandwidth after downconversion to avoid the aliasing of out-of-channel blockers and noise due to the following sampling operation. By increasing the order and therefore the power consumption of the analog LPF, the sample rate, the resolution, and therefore the power dissipation of the ADC, can all be decreased and vice versa.

- The Variable Gain Amplifier (VGA) provides programmable gain so that the signal processed by the baseband circuits appears to be at a constant level at the input of the ADC regardless of the actual signal power received at the antenna. The VGA is normally driven by an AGC algorithm, as discussed in paragraph 3.5. The gain range to be covered depends on the minimum and maximum signal that can be received for a certain wireless standard.

3.2   Baseband Trade-Offs for Analog to Digital Conversion

According to the implementation strategy, careful attention is needed regarding the influence on the required baseband specifications on the system. Channel-selection schemes must be able to satisfy the system, either at Radio Frequency (RF) and Intermediate Frequency, and digital requirements. A link budget analysis is required that is normally based on the following key system level parameters:

- **Sensitivity** defines the lowest input RF signal that must be detected and distinguished by the receiver with acceptable quality.

- **Blockers, spurs, and image interferers** are RF signals transmitted into the air by other wireless devices and can penetrate and either saturate the receiver

or interfere with the signal being received. Understanding the wireless applications that coexist in the frequency spectrum surroundings the band of interest is a must.

- The **Inter-Symbol Interference** (ISI) leads to higher Bit Error Rate (BER) in the detection of random waveforms that are transmitted through band-limited channels. The problem of ISI is particularly troublesome in wireless communication because the bandwidth allocated to each channel is fairly narrow.

A link budget analysis uses these parameters, normally specified by the wireless standard, to determine the receiver lineup and the requirements of various receiver blocks. This typically involves calculations for gain, noise figure, filtering, Intermodulation products, and input 1dB compression (P1dB).

In the following, we give a short analytical description for each one of these trade-offs. Furthermore, following the approach in Jussila and Halonen (2004) and Seo et al. (2003), we provide an estimation of the total power consumption and a way to minimize it. Only all-pole filters and Nyquist-rate ADC are discussed here.

3.2.1 Number of poles for the LPF

Let us assume that the input signal is band-limited (F_b), as shown in Figure 3.2. As discussed in Maloberti (2007), if F_s is the ADC sampling frequency, possible spurs in the frequency interval $[F_s/2 \rightarrow (F_s - F_b)]$ are not critical as their images fold outside the band of interest. On the other hand, the spurs inside the frequency range above $[(F_s - F_b) \rightarrow F_s]$ threaten the signal spectrum and must be properly rejected up to the so called stop-band attenuation A_{SB}. Let us take into account the attenuation of a Butterworth transfer function. When $F \gg F_b$, the transfer function can be approximated to:

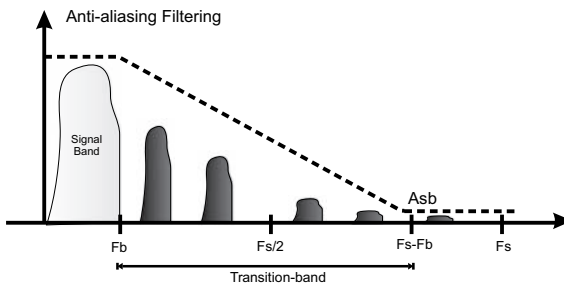$$A_{dB}(F) \approx 20 n_P \log\left(\frac{F}{F_b}\right) \qquad (3.1)$$

Figure 3.2. Aliasing effect and anti-aliasing filter requirements.

where n_P is the number of poles. If we define the filter transition-band T_B as the one included between F_b and $F_s - F_b$, it is possible to calculate the roll-off r_B $[dB/dec]$ of a Butterworth transfer function as:

$$r_B(F_s, F_b) = A_{dB}(F_s - F_b) - A_{dB}(F_b) = 20 n_P \log \left(\frac{F_s - F_b}{F_b} \right) \quad (3.2)$$

When we put together Equations (3.2) and (3.1), we obtain the minimum required filter order for a given F_s and F_b:

$$n_P(F_s, F_b) \geq \left\lceil \frac{A_{SB,dB}}{T_B 20 \log[(F_s - F_b)/F_b]} \right\rceil \quad (3.3)$$

that clearly shows how the filter order is directly proportional to the required stop-band attenuation and signal bandwidth whereas an higher sampling frequency relaxes the selectivity specifications at the expenses of the ADC.

3.2.2 ADC dynamic range

The dynamic range of the ADC is the key criteria that defines the range of voltages that can be digitized with acceptable quality. The dynamic range is connected to the number of bits n_b by the following equation:

$$DR = 6.02 n_b - 1.25 + 10 \log \left(\frac{F_s}{F_b} \right) \quad (3.4)$$

where the ratio F_s/F_b is the eventual oversampling ratio α_p. The number of bits defines the lowest voltage that can be detected by the ADC and this Least Significant Bit (LSB) Δ should be normally much lower than received signal so that the quantization noise corrupts the SNR at the ADC output negligibly. The mean squared quantization noise of an n_b bits ADC is given by:

$$\sigma_Q = \frac{\Delta^2}{12} = \frac{1}{12} \left(\frac{FS}{2^{n_b}} \right)^2 \quad (3.5)$$

The degradation of SNR for a 3–6 bit ADC is plotted in Figure 3.3. For example, the quantization noise from a 5 bit ADC is below 0.1 dB for input SNR below 0.5 dB. A good criteria is to set the quantization noise at least 20 dB below the signal level (Razavi, 1999). A good way to relax the ADC DR is also to use a certain level of oversampling. If α_p is about 6 dB, i.e. the sampling frequency is four times Nyquist, in the case of UMTS/FDD, a 4 or 5 bits would be sufficient for a performance degradation of 0.1–0.2 dB without out-of-channel signals (Vejlgaard et al., 1999). This subsection explains how the required dynamic range of the ADC is calculated. The proper DR for the ADC is the result of a trade-off with the baseband variable gain. The gain should
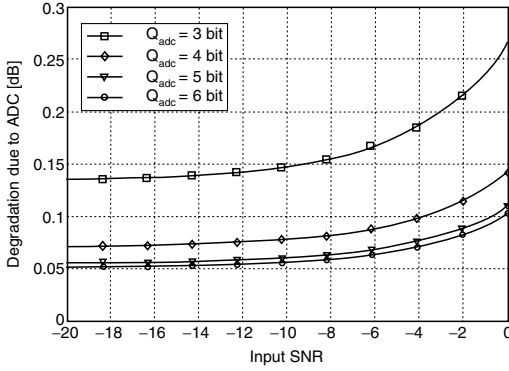
Figure 3.3. Performance loss due to quantization in the ADC. (From Vejlgaard et al., 1999.)

be big enough to minimize the ADC number of bits in case a small signal is received, but not so big to avoid strong nonlinearity to appear throughout the receiver when large signals are received. Therefore, the ADC requirements must be determined for two signal conditions: at sensitivity and when a large interferer (blocker) is present.

3.2.2.1   The Sensitivity Level

As explained in Razavi (1998), the minimum input power that can be received with acceptable quality is given by:

$$S_{min}|_{dBm} = SNR_{min}|_{dB} + F|_{dBm} \qquad (3.6)$$

where S_{min} is the minimum input level that achieves a minimum Signal to Noise Ratio (SNR_{min}), normally called sensitivity level, and F is the total integrated noise power, also called *noise floor*. It is possible to calculate F as:

$$F|_{dBm} = P_{RS}|_{dBm/Hz} + NF|_{dB} + 10\log(B) \qquad (3.7)$$

where NF is the noise figure of the receiver, B the channel bandwidth across whom the overall signal power is distributed, and P_{RS} the source resistance noise power that, assuming conjugate matching at the input, is given by the Boltzmann's constant:

$$P_{RS} = kT|_{dBm} = -174\,dBm/Hz \qquad (3.8)$$

Let us give an example considering the Digital Enhanced Cordless Telecommunications (DECT) standard: the sensitivity level is here specified as $S_{min} = -95$ dBm for a channel bandwidth given by $B = 1.152$ MHz. The minimum SNR to obtain a $BER < 10^{-3}$ is estimated as being $SNR_{min} = 14$

dB. That corresponds to a NF of 4.38 dB for our Digital Enhanced Cordless Telecommunications (DECT) receiver and to a total noise power $F = -109$ dBm.

3.2.2.2   Scenario with No Blockers

Let us assume first that all the interferers are well attenuated by the LPF and no large blockers are present. The required programmable gain range at baseband is normally calculated using the reference sensitivity and maximum input level test cases.

In case there is no blocker, the calculation of the maximum gain requirement is shown in Figure 3.4 starting from the sensitivity level S_{min}. The margin below the noise floor F is calculated considering that the baseband part should have a small contribution to the receiver noise figure (NF_{RX}) compared to the noise figure of the RF part (NF_{RF}) and this mainly for power consumption reasons. For example, if NF_{RX} is 7 dB and budget 6 dB (80% overall) is foreseen for the RF part, then there is 0.12 dB left for the ADC. In general, the margin below F of the receiver as a function of the NF_{RX} and NF_{RF} is given by:

$$MbelowF_{no-bl} = 10 \log \left(\frac{1}{1 - 10^{\frac{NF_{RF}-NF_{RX}}{10}}} \right) \tag{3.9}$$
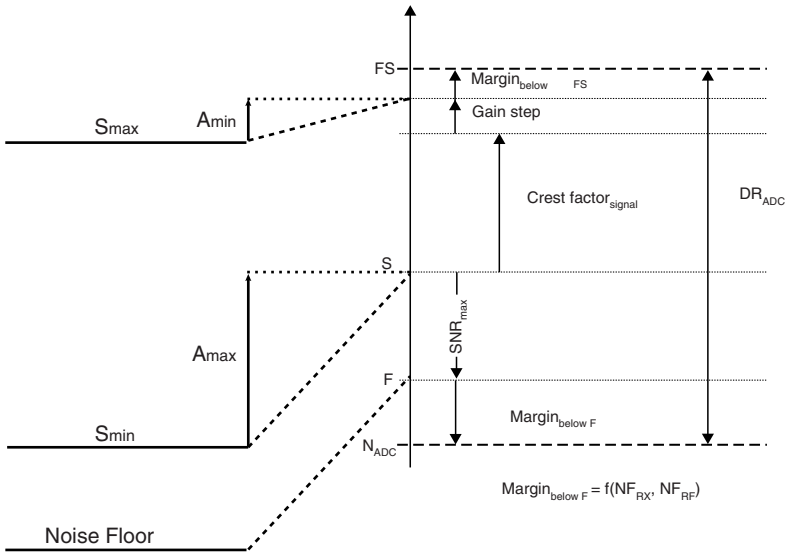

Figure 3.4.   Minimum required ADC dynamic range without blockers.

In the upper part, the crest factor of the signal is added and we assume that the AGC maps the signal on the ADC input range with an accuracy equal to gain step. Finally we include a margin below the Full Scale (FS) of the ADC.

In this case, the maximum and minimum gain settings are defined as follows:

$$\begin{cases} A_{max} = \sigma_Q + SNR_{min} + Mbelow F_{no-bl} - S_{min}; \\ A_{min} = FS - Mbelow FS - S_{max}. \end{cases} \tag{3.10}$$

The SNR at the input and the output of the ADC can be expressed as:

$$\begin{cases} SNR_{in} = P - Mbelow F_{no-bl} \\ SNR_{out} = P - (\sigma_Q + Mbelow F_{no-bl}) \end{cases} \tag{3.11}$$

where P is the signal power amplified by the receiver chain. Let us give an example. In the GSM standard, the channel of interest is anywhere between -102 dBm (S_{min}) and -15 dBm (S_{max}) for 87 dB of input dynamic range. Assuming the resolution of our ADC is $n_b = 14$ bits and $FS = 1$ dBm, the quantization noise σ_Q is -85 dBm. For acceptable BER, the GSM standard requires 9 dB of SNR_{min}. In order to limit the impact of the quantization noise on the output SNR to 0.1 dB loss, the margin below F is set to be 16 dB. This yields to a maximum gain $A_{max} = 42$ dB. For large inputs, if the margin below FS is set to be 6 dB, $A_{min} = 10$ dB.

3.2.2.3 Scenario with Strong Blockers

In presence of a blocker, the calculation is more complicated and it is shown in Figure 3.5. The upper end of the Dynamic Range (DR) is defined as the maximum input level in a two-tone test for which the third-order Inter-Modulation (IM) products do not exceed the noise floor. This can be analytically expressed as in Razavi (1998):

$$P_{in,max}|_{dBm} = \frac{2P_{IIP3} + F}{3} \tag{3.12}$$

where P_{IIP3} is the Input Intercept third-order power and can be defined as:

$$P_{IIP3} = \frac{3P_{IN} - P_{IM,in}}{2} \tag{3.13}$$

where $P_{IM,in}$ is the input referred level of the third-order IM (IM3). Finally, it is possible to define a Spurious-Free Dynamic Range (SFDR) as:

$$SFDR = \frac{2(P_{IIP3} - F)}{3} - SNR_{min} \tag{3.14}$$

that represents the maximum relative level of interferers that a receiver can tolerate while producing an acceptable signal quality from a small input level.
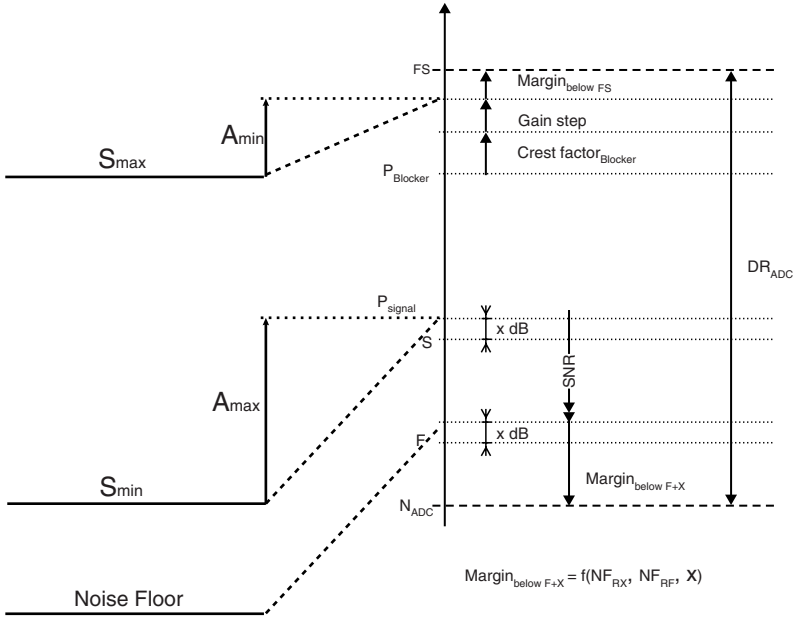
Figure 3.5.   Minimum required ADC dynamic range with blockers.

The blockers are defined in different receiver tests for a certain communication standard. In these tests the desired signal is most of the time at a certain level above the sensitivity level (let us say x dB above the sensitivity level). The margin below F in case blockers are present is then given by:

$$Mbelow F_{bl} = Mbelow F_{no-bl} + x|_{dB} \qquad (3.15)$$

where we assume that the contribution of the quantization noise to the overall noise figure of the receiver stays the same at all receiver test signal power levels. After downconversion to the baseband, the in-channel signal power P_{SN} contains the wanted signal P_{signal} and the thermal input noise generated in the receiver $F_{blockers}$. Therefore, the signal at the ADC input is given by the sum of P_{SN} and the residual out-of-channel blockers after the analog low-pass filtering, whose power is P_{BL}. The dynamic range of the ADC is then given by:

$$DR_{ADC,dB} = P_{SN} + \xi_{SN} + P_{BL} + \xi_{BL} \qquad (3.16)$$

where ξ_{SN} and ξ_{BL} are respectively the crest factors of the in-channel signal and the out-of-band residual blockers. In Equation (3.16) we are assuming that the maximum instantaneous in-channel and out-of-channel signal amplitudes are summed. Though the probability that this may occur is very small (Jussila

and Halonen, 2004). Therefore, it may be possible to decrease the dynamic range in the ADC without an unacceptable degradation in the signal quality.

3.2.2.4 Baseband Variable Gain

The variable gain range at baseband is given by:

$$\Delta G_{BB} = 20 \log \left(\frac{A_{max}}{A_{min}} \right) - \Delta G_{RF} \tag{3.17}$$

where ΔG_{RF} is the variable voltage gain in the RF section and $A_{RX,max}$ and $A_{RX,min}$ are respectively the maximum and minimum voltage gain of the receiver. Therefore, to calculate the required variable gain range in the receiver we need to find out the minimum and maximum in-channel powers referred to the antenna connector.

3.2.3 Baseband power consumption estimation

In order to have an instant feedback on the power consumption of the baseband section according to different level of filter selectivity and ADC dynamic range, we exploited the two typical figure of merits for filters and ADC. The power consumption of an analog low-pass filter can be approximated to be linearly dependent on the number of poles n_P:

$$P_{LPF} = P_{pole} n_P (f_s, f_B) \tag{3.18}$$

where P_{pole} is the power dissipation per pole in an all-pole low-pass filter. On the other hand, the power consumption of a Nyquist rate ADC can be approximated as follows:

$$P_{ADC} = E_{conv} f_S 2^{ENOB} \tag{3.19}$$

where E_{conv} is the energy required per conversion step and the effective number of bits is given by:

$$ENOB = \frac{SNDR - 1.76}{6.02} \tag{3.20}$$

where SNDR is the Signal to Noise and Distortion ratio of the ADC. The overall baseband power consumption is then given by:

$$P_{BB} = P_{LPF} + P_{ADC} = P_{pole} n_P (f_s, f_B) + E_{conv} f_S 2^{ENOB} \tag{3.21}$$

where the power of the AGC and the digital filtering are omitted for simplicity. Figure 3.6 shows some trade-offs between filter order and sampling frequency for different standard. For simplicity, an estimation of the P_{pole} for each standard has been made based on simulations results (Table 3.1) and a E_{conv} of
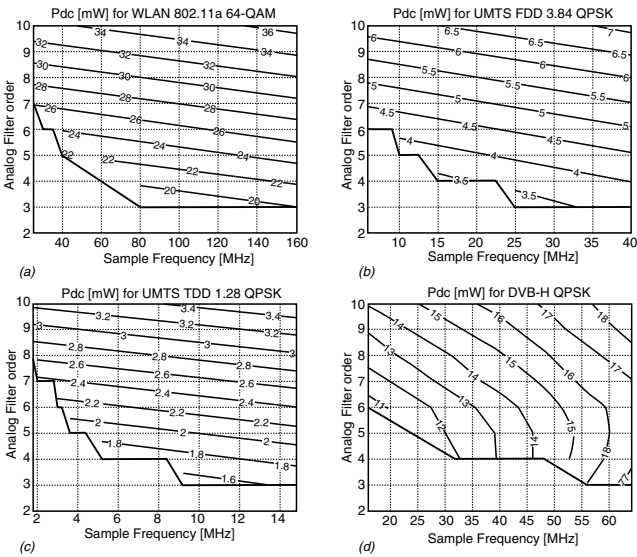
Figure 3.6. Trade-off between F_S and n_P for Nyquist rate ADC at different standards. (a) WLAN 802.11a, (b) UMTS FDD 3.84, (c) UMTS TDD 1.28, (d) DVB-H QPSK. (From Driessche 2005.)

Table 3.1. Power per pole of channel select filter for different standards.

Standard	$f_B[MHz]$	$P_{pole}[mW]$
5 GHz WLAN 802.11j	4.15	1.3
5 GHz WLAN 802.11a	8.33	2.4
5 GHz WLAN 802.11n	16.6	3.52
DVB-H	3.8	1.1
UMTS 3.84 Mcps	1.92	0.6
UMTS 1.28 Mcps	0.64	0.31

1 pJ is taken into account for the ADC. The figure helps to define the lowest power solution and the relative filter selectivity needed and ADC sampling frequency. For example, ideally for a WLAN 802.11a, the lowest power possible for the baseband analog circuits and ADC is 18 mW, which corresponds to a third-order filter and 80 MS/s of F_s.

3.3   Multistandard Analog Baseband Specs

The basic purpose of a *single standard* receiver is to detect and deliver a RF signal from the antenna to the ADC while maintaining signal quality as much as possible. In order to determine the individual specifications of the receiver blocks a link budget analysis is usually performed. Obviously the complexity

of this system analysis quickly outgrows when we deal with *multimode multi-standard* receivers: the basic idea here is to share as much hardware as possible for different wireless standards and therefore provide a *range* of requirements for each analog block.

A link budget analysis for a SDR front end provides a range of input specifications that allow to cover all the foreseen standards with optimum power consumption in each mode. Assuming that our flexible receiver provides a NF in the range of 4–8 dB, a gain range between 10 and 90 dB and an overall IIP3 of about −9 dBm (Craninckx et al., 2007), the range of requirements for the baseband section is the result of an optimal distribution of gain, noise, and linearity throughout the receiver blocks.

The baseband signal processing will be normally provided by a low-pass filter with a pass-band that is tunable over several decades. The filter should enable the channel of interest to be digitized at the required SNR for acceptable demodulation and therefore limit the DR presented at the ADC input. In addition to that, the low-pass filter allows sampling of the signals at a reasonable rate to achieve power dissipation consistent with mobile requirements. In order to accommodate the bandwidths from the Bluetooth to the WLAN 802.11n, this flexible baseband filter must cover a relatively wide range of cut-off frequencies, from a few hundreds of KHz up to 20 MHz. Various standards have different requirements for channel selectivity. Therefore, the receive filter transition bandwidth should be programmable. This feature can then also be used to save power in the presence of interferers weaker than the worst case for the given standard. In addition to that, an adaptive Input Referred Noise (IRN) level may lead to a further power saving when a wireless standard with lower SNR specifications has to be selected.

On the other hand, the ADC and DSP should relieve the analog front end from the traditional burdens of variable gain and filtering. In a flexible direct conversion receiver, the baseband section pass-band should be widely variable. To serve the variety of cellular and WLAN standards, the ADC should also be reconfigurable; for instance, GSM reception generally needs 85 dB DR in a $200\,\text{kHz}$ bandwidth and $10\,\text{MHz}$ sample rate, whereas 802.11g reception needs a DR of 8 bits across the Nyquist band at $40\,\text{MHz}$ rate Wolf (2005).

3.4   Multimode Low-Pass Filter

Whereas noise and nonlinearity in the RF front end determine the sensitivity of a wireless receiver, the filters govern its selectivity that is, its ability to pick out a signal of interest in a frequency band, while rejecting all the other nearby signals present in that band. The channel-select filter must satisfy different requirements. The first and most important is selectivity. A filter with a sharp cut-off frequency should select the desired channel and attenuate all other adjacent users. The frequency response of the such a filter depends on the

required accuracy and it is usually the result of an accurate power trade-off with
the ADC's SNR. Furthermore, an active implementation of the filter must itself
be low noise so as not to degrade the overall receiver noise figure, and it must
have wide dynamic range so that out-of-band interferers, prior to filtration, do
not create intermodulation distortion which falls in the pass-band. Since the
folding of spurs into the pass-band is also named aliasing, this *continuous-time
filter* may be called *anti-aliasing* filter.

3.4.1   Filter selectivity

Adjacent Channel Selectivity (ACS) is a measure of a receiver's ability to
receive a signal at its assigned channel frequency in the presence of an adjacent
channel signals at a given frequency offset from the center frequency of the
assigned channel. ACS results then in the ratio between the filter attenuation
on the assigned channel frequency and the adjacent channels. The selectivity
requirements comes out from a detailed analysis of the blockers and interferers
characteristics for each standard. The filtering specifications are usually not
given in the form of rational functions, but as lines or curves that give, for
example, max and min attenuation. These lines determine the so-called speci-
fied curve. A channel selection filter mask is derived for the different considered
standards (Figure 3.7). Tables 3.2 and 3.3 show the required adjacent channel
selectivity as well as the in- and out-of-band blocking attenuations for each
standard we consider critical for our SDR receiver in more detail. In practice,
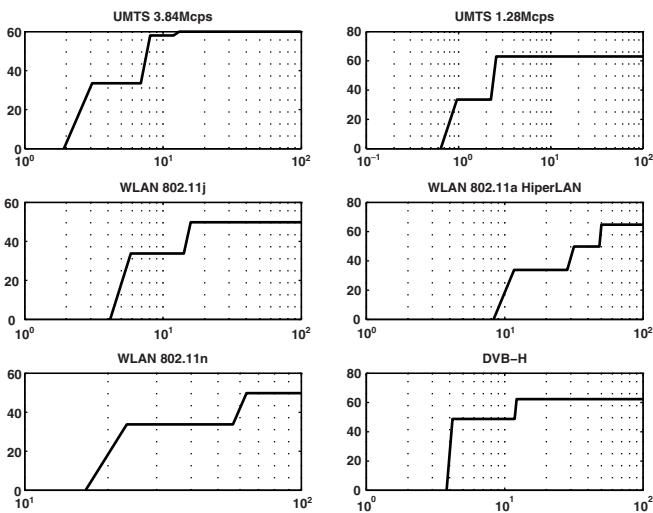
Figure 3.7.   Required adjacent channel selectivity for each of the standards evaluated.

Table 3.2. Filter mask requirements for different 5 GHz WLAN standards.

5 GHz WLAN 802.11j		5 GHz WLAN 802.11a		5 GHz WLAN 802.11n	
Band [MHz]	Att. [dB]	Band [MHz]	Att. [dB]	Band [MHz]	Att. [dB]
0–4.15	0	0–8.3	0	0–16.6	0
5.85–14.15	33.8	11.7–28.3	33.8	23.4–56.6	33.8
15.85–24.15	49.8	31.7–48.3	49.8	63.4–96.6	49.8
–	–	>50	64.8	–	–

Table 3.3. Filter Mask requirements for UMTS and DVB-H.

UMTS FDD 3.84 Mcps		UMTS TDD 1.28 Mcps		DVB-H	
Band [MHz]	Att. [dB]	Band [MHz]	Att. [dB]	Band [MHz]	Att. [dB]
0–1.92	0	0–0.64	0	0–3.81	0
3.08–6.92	33.5	0.96–2.24	33.5	4.2–11.81	48.8
8.08–11.92	58	2.56–3.84	63	12.2–19.81	62.3
>15	60	>6.4	63	–	–

the specifications of the filter may be given in terms of the cut-off frequency f_c, the maximum allowable deviation (error) A_{max} in the pass-band, the stop-band edges, and the minimum attenuation A_{min} in the stop-band.

The next step in the filter design is the determination of the permitted rational function that best approximates the specified curve, i.e. that satisfies the conditions set by the specified mask. Usually the complexity (and consequently the cost) of the circuit increases with the order of the permitted function that is selected. It is therefore necessary to determine the simplest permitted function that satisfies the specifications according to the following criteria:

- **Frequency domain**
  If we accept a small error in the pass-band and a nonzero transition band, we need a rational function $F(s)$ whose magnitude will approximate the ideal response as closely as possible. A suitable magnitude function can be of the form:

$$|F(j\omega)| = \frac{1}{\sqrt{1 + \varepsilon^2 w(\omega^2)}} \qquad (3.22)$$

where ε is a constant between zero and one ($0 < \varepsilon < 1$), according to the accepted pass-band error, and $w(\omega^2)$ is a function of ω^2 such that:

$$\begin{cases} 0 \leq w(\omega^2) \leq 1 \\ 0 \leq \omega \leq 1 \end{cases} \qquad (3.23)$$

and which increases very fast with increasing ω, for $\omega > 1$, remaining much greater than one outside the passband. In general, the numerator may be a constant other than unity, which will influence the gain (or attenuation) at DC.

- **Time domain**
  The system-level design of low-pass filters located in the signal path of frequency-domain equalization systems, should meet not only the spectral specification, but also the ISI specifications. Attenuation of high-frequency components of a periodic square wave in a low-pass filter can indeed distort a signal heavily affecting the BER. Figure 3.8 shows how different channel-select filters can actually degrade in a different way the BER performance. However, the ISI cannot be directly related to BER and actually BER simulations may require a very long computation time. If we look at the output of a low-pass filter, we notice the output exhibits an exponential tail that becomes more significant as filter bandwidth decreases. This occurs because a signal cannot be both time limited and bandwidth limited. Both the duration and shape of the overall impulse response determine the amount of ISI. Yet, with a given response, the amount of interference is also dependent on the synchronization location at the receiver. The ISI caused by
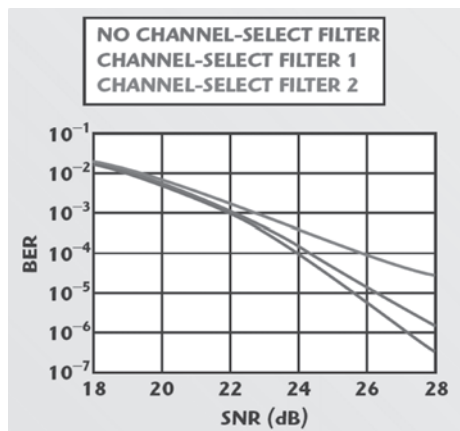
Figure 3.8. BER degradation caused by channel filter insertion. (From Debaillie et al. 2001.)
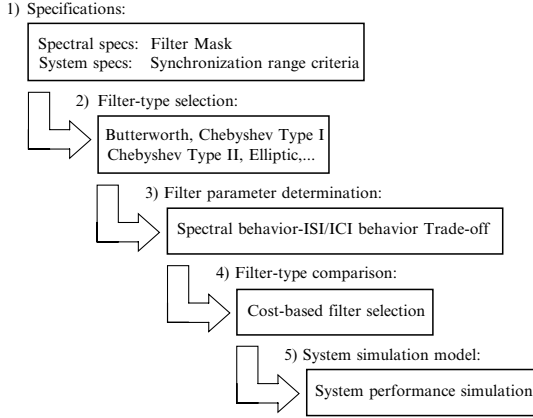
Figure 3.9. System-level filter design methodology.

a filter can be approximated as the sum-of-squares value of the distortion of the impulse response of the filter at optimal sampling instants nT_D (Jussila, 2003):

$$ISI = \frac{\sum_{n=-\infty, n\neq 0}^{\infty} \left[h(nT_D)^2 \right]}{h(0)^2} \tag{3.24}$$

No ISI occurs if the impulse response has a value of zero at time instants of nT_D. In order to find the best filter transfer function in terms of BER, the model proposed in Debaillie et al. (2001) is exploited. It allows to analyze given filters with respect to ISI and synchronization location, thus providing direct insight in the cause of the performance degradation. Figure 3.9 resumes the design methodology.

In zero-IF receivers, the overall channel-select filtering is typically the result of a careful partitioning between the analog and the digital domain. The transfer of some amount of channel-select filtering from the analog to the digital domain requires a higher dynamic range, and possibly a higher sample rate in the following ADC but requires at the same time higher power consumption. On the other hand, digital filters having linear phase can be easily implemented at lower costs: digital filters do not need time-constant tuning, are not affected by aging, and do not suffer from component mismatches as their analog counterparts do. Therefore, Finite-Impulse Response filters are commonly used to achieve a sufficient attenuation of the adjacent channel because much more complicated filters having higher selectivity without ISI can be implemented in the digital domain. A proper trade-off between analog and digital filtering is needed.

3.4.2   Filter noise and linearity

Noise and linearity specifications for a flexible baseband filter are the result of an accurate trade-off that involves the in- and out-of-band blockers level, the receiver's total gain and NF, and the total power consumption for each wireless standard involved. A careful system-level analysis determines first the worst case input referred noise for the entire baseband section as a function of the RF gain. Therefore, the same is done with large signals that might generate distortions: the minimum required Input Intercept Third-Order Power is calculated as a function of the RF gain. The best trade-off results in a range of input specifications that allow the flexible transceiver to achieve multistandard compliancy and, of course, defines the required level of flexibility for each analog circuit part of the receiver chain.

The *noise performance* of the receiver defines its sensitivity by limiting the lowest input RF power that can be detected. At low amplitude levels, when the filter's output is constant regardless of the input, we have reached the so-called noise floor. Noise is mainly due to thermal motions and quantized current flows in the circuit components, which add a random fluctuation to the deterministic output signals (Razavi, 1998). When noise and signal become equal in size, we are close to the borderline below which makes the output is useless. It is a common design challenge to push the noise floor to an acceptable minimum for a given application. Let us consider the receiver's block scheme in Figure 3.10. To determine the input-referred noise voltage for a multimode low-pass filter, we first need to estimate the voltage gain in the RF part of the receiver for each standard. The NF for the complete receiver is given by applying the Friis formula:

$$NF_{RX} = NF_{RF} + \frac{NF_{BB} - 1}{A_{RF}^2} \tag{3.25}$$

where NF_{RF} and A_{RF} are respectively the noise figure and gain of the RF section and NF_{BB} is the noise figure of the analog baseband. The noise figure of the baseband section can be expressed with respect to a source impedance R_S as:
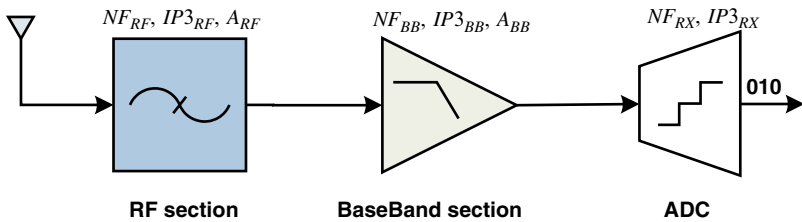
Figure 3.10.   Receiver's block scheme.

$$NF_{BB} = \frac{SNR_{BB,in}}{SNR_{BB,out}} = 1 + \frac{\bar{v}_{n,out}^2}{4kTR_S A_{BB}^2} = 1 + \frac{\bar{v}_{n,in}^2}{4kTR_S} \qquad (3.26)$$

where k is the Boltzmann's constant and $\bar{v}_{n,in}^2$ is the input referred noise power specified for a 1 Hz bandwidth at a given frequency.

The maximum allowed RF gain $A_{RF,max}$ is determined so that the output stage of the last RF block does not saturate under the defined specifications of the relative standard. Therefore *linearity considerations* are here involved: large signal operation of transistors may degenerate the filter's performance by formation of distortion components at frequencies multiple of the input signal frequencies. The output may saturate to constancy but in most applications the limit for acceptable performance is reached long before that. Linearity is mostly characterized by two key performance parameters: Input Intercept third-order power and IM3. These two parameters are the result of a two-tone analysis in which two in-band signals are subjected to the receiver or one of its components. The tones mix due to the nonlinear elements in the receiver and generate products that can be used to characterize the extent of the nonlinearity. The amplitude of the Input Intercept third-order power (IIP3) for the overall receiver is determined by:

$$\frac{1}{A_{IP3,RX}^2} = \frac{1}{A_{IP3,RF}^2} + \frac{A_{RF}^2}{A_{IP3,BB}^2} \qquad (3.27)$$

where $A_{IP3,RF}$ and $A_{IP3,BB}$ are respectively the Input Intercept Third-Order Power (IIP3) of RF and baseband sections, as specified in Figure 3.10.

Therefore it seems clear that one of the most important RF design parameters that directly influence the baseband design is the RF gain (Figure 3.11).
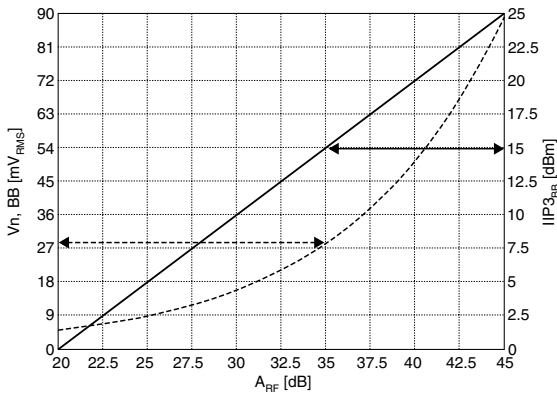
Figure 3.11. Input Referred Noise voltage and 3rd order InterModulation at baseband as function of the RF gain.

Table 3.4. Input specifications for a flexible baseband low-pass filter intended for a multi-standard zero-IF receiver.

Standard	BW_{tot} [MHz]	Min. attenuation [dB]	$v_{n,in}$ $[\mu V_{rms}]$	IIP3 [dBm]
Bluetooth	1	30 @ 1.5 MHz	96–183	17.3
UMTS TDD	1.28	63 @ 3.84 MHz	52–104	18.4
UMTS FDD	3.84	58 @ 11.92 MHz	51–106	20.42
DVB-H	7.6	49.8 @ 19.8 MHz	62–127	17.9
WLAN 802.11a	16.66	49.8 @ 48.6 MHz	53–105	21.5
WLAN 802.11n	33.2	49.8 @ 96.6 MHz	75–149	21.5

If the RF gain is increased, the noise requirements on the baseband section are relaxed, as clear from (3.25) and (3.26). This is because the RF gain amplifies the desired signal and hence the noise added by the baseband circuit becomes less influential. On the other hand, increasing the RF gain will also amplify the blockers and hence a circuit with better linearity is required to prevent the intermodulation products from corrupting the desired signal (3.27). A good approach is to determine A_{RF} by the largest blocker in the intermodulation test, move more stringent linearity requirements to the baseband so determining an higher distortion coming out from the RF section compared to the baseband. Finally, the noise levels can be determined. This is to relax the noise specifications on the baseband analog section that otherwise would be very power consuming. Table 3.4 shows the baseband specifications for all the standards we want to be compliant in a SDR front end.

3.4.3   Filter flexibility planning

Designing such a flexible analog baseband section makes sense as far as a wide range of requirements has to be covered. However, the resulting conventional Continuous Time (CT) filter will require so many degrees of programmability that might become no longer practical. In this section we explore the intrinsic limitation for designing a flexible analog filter.

3.4.3.1   Filter Cut-Off Frequency Tuning

Covering a wide range of cut-off frequencies with the same RC-based filter implies a compromise between accuracy (components size) and cost (silicon

(a) C constant   (b) R constant
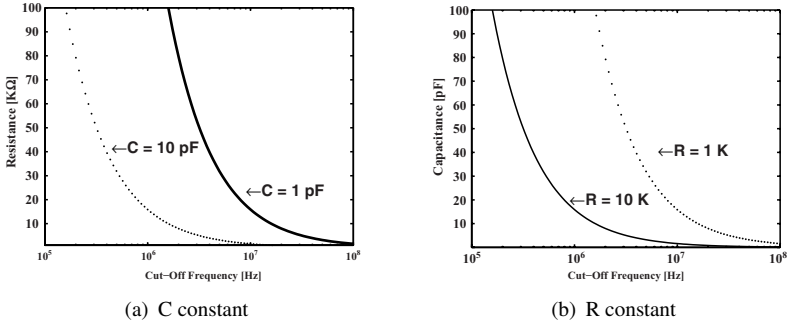
Figure 3.12. We exemplify possible trade-offs for an ideal integrator, keeping first constant the capacitors (a) and then the resistors (b).

area) for both resistors and capacitors. In this work, we achieve a coarse frequency tuning (to cover a large frequency range with poor accuracy) by modifying the resistors values.

For example, let us consider from simplicity an ideal integrator: Figure 3.12(a) shows that in order to cover the frequency range between 2 and 20 MHz keeping constant the capacitor value (1 pF), we would require the resistor to vary from 8 to 80 KΩ, which are reasonable values for integration in modern CMOS processes. If we want to cover the same range of frequency keeping constant the resistor value (1 KΩ), as shown in Figure 3.12(b), we would require a maximum capacitor value of 80 pF. This is why in our design, we achieve a coarse frequency tuning (to cover a large range of frequency with poor accuracy) by modifying the resistors values. Once the maximum and minimum cut-off frequency, $f_{co,max}$ and $f_{co,min}$ respectively, are defined, the minimum number of bits needed to cover this frequency range with a frequency step $f_{co,step}$ is given by:

$$n_{ct} = \left\lceil \log_2 \left(\frac{f_{co,max}}{f_{co,min}} \right) \right\rceil \qquad (3.28)$$

where $\lceil .. \rceil$ is the ceiling function and where we have chosen $f_{co,step} = f_{co,min}$ to minimize the circuit complexity. This solution leads to a system with a discrete set of bandwidths placed at a minimum distance of $f_{co,step}$. By changing the resistor values in an op-amp RC filter, the load impedance of the integrator op-amp also changes. Therefore, concurrently, power scalability can be obtained by using a proper op-amp architecture that somehow adapts its power consumption to the current load impedance. On the other hand, to achieve fine frequency tuning, the capacitance value is modified by means of a capacitor

array. The relative error ε by using a capacitor unit δC to correct the cut-off frequency with a nominal capacitance value C_{nom} is given by (Corsi et al., 2007):

$$\varepsilon = \pm \left(\frac{\delta C}{2C_{nom}} \right). \tag{3.29}$$

It can be easily demonstrated that the minimum number of bits needed by the capacitor array to fine-tune the cut-off frequency for an RC process deviation of ξ and relative error ε is given by:

$$n_{ft} = \left\lceil \log_2 \left| \frac{\xi}{\varepsilon(1 - \xi^2)} + 1 \right| \right\rceil. \tag{3.30}$$

3.4.3.2 Filter Input Referred Noise Tuning

The integrated noise in active-RC filters is mainly determined by the kT/C noise. While performing a coarse frequency tuning, the input integrated noise $v_{n,in}$ remains constant as we are changing the resistance value. On the other hand, $v_{n,in}$ increases by lowering the capacitance value. This is a principle we want to take advantage of: the power dissipation may indeed be reduced by increasing the noise floor (Krishnapura and Tsividis, 2001; Tsividis et al., 2003; Palaskas et al., 2004; Ozgun et al., 2006). When the load capacitance of an integrator op-amp is reduced, its driving capabilities can be reduced and power savings can thus be achieved by using a proper reconfigurable op-amp together with a programmable array of capacitors. For n_s noise steps, the number of bits needed for reconfigurability is $n_{nt} = \lceil log_2(n_s) \rceil$. If $\mathbf{hn} = [hn_{n_{nt}-1}, ... hn_1, hn_0]$ is the noise input digital word, the frequency step can be redefined from (3.28) as follows:

$$f_{co,min} = f_{co,step} = \frac{f_{co,max}}{2^{n_{ct}}} \left(\sum_{k=0}^{n_{nt}-1} hn_k 2^k + 1 \right) \tag{3.31}$$

As both n_{ft} and n_{nt} act on the capacitance value, we define the total number of bits needed to drive the capacitor array as

$$n_{cap} = n_{ft} + n_{nt}. \tag{3.32}$$

3.4.3.3 Filter Selectivity Tuning

High-order filter transfer functions can be implemented by cascading biquadratic sections: this is a viable option for low-cost design since it allows power and area savings if compared with double amplifier approaches, assuring a good level of controllability as well. Furthermore, this approach is relatively easy and intrinsically flexible. Bypassing a biquadratic section leads to decrease the order of the filter and saving power by switching off the correspondent biquad

op-amp. This feature can be used in case less adjacent channel selectivity is required. As this operation is performed while a signal is being received for a certain standard, the biquadratic cell is required to switch on/off quickly enough according to the standard specifications.

3.4.4 Cascade of biquadratic sections

After the signal is downconverted to the baseband, it must be filtered, amplified, and digitized, but not necessarily in that order. Consider the interface between the mixer and the first baseband stage. We make three observations:

1 At this point the signals are still quite small (in the range of tens of *microvolts*) and the interferers quite large (e.g. 60 dB above the signal level) Thus, both the noise and the nonlinearity are critical;

2 To avoid lowering the voltage gain of the mixer, must exhibit a relatively high input impedance.

3 Resistive feedback techniques suffer from severe trade-offs among noise, input resistance, and power dissipation. Moreover, high-input impedance amplifiers exhibit substantial noise because of the contributions of the two amplifiers.

With the above in mind, we realize that the design of the LPF may not be optimal if not preceded by an accurate requirements distribution on each biquadratic section.

At the system level, the filter is described specifying filter type and order, cut-off frequency, gain, load impedance, maximum in-band Root Mean Squared (RMS) input noise, and maximum IM3 (computed for maximum input signal amplitude) or, equivalently, minimum IIP3 in the filter bandwidth. Given the poles of the transfer function, an optimal order of biquad cell cascade is selected based on noise, linearity, and power consumption criteria. The cascade optimization is very general and does not depend on a specific cell architecture. In order to back-annotate data on power consumption and feasibility, an accurate model has to be provided for the specific biquad cell. The filter transfer function of a cascade of N biquad cells can be generally written as:

$$H(s) = H_1(s)H_2(s) \cdots H_N(s) \tag{3.33}$$

where $H_i(s)$ are biquad transfer functions of the form:

$$H(s) = \frac{K\omega_0^2}{s^2 + (\omega_0/Q)s + \omega_0^2} = Kh(s) \tag{3.34}$$

where K is the DC gain, Q is the quality factor, ω_0 is the pole frequency and subscripts increase going from the input to the output. Noise is assumed

to be white (thermal noise) at least in the filter bandwidth and an improved approximation over the basic Friis noise formula is exploited. The noise power at the output of the filter in its bandwidth B can be expressed as:

$$N_{out}^B = \sum_{i=1}^{N} IRN_i^2 \int_B \prod_{j=i}^{N} |H_i(f)|^2 \approx \sum_{i=1}^{N} IRN_i^2 \prod_{j=i}^{N} \alpha_j^2 B \qquad (3.35)$$

where IRN^2 is the input referred noise power spectral density (PSD) of each biquad in the filter bandwidth. Traditionally, the total output noise power is computed by substituting each $|H_i|$ with a function equal to a constant α_i over the equivalent noise bandwidth and zero elsewhere. In the Friis formula, $\alpha_i = |H_i(0)|$. We define an Effective in-Band Gain (EBG) G_i as:

$$G_i^2 = \frac{\int_B |H_i(f)|^2 df}{B}. \qquad (3.36)$$

Setting $\alpha = G_i$ allows capturing the increased amount of noise power in the filter bandwidth due to higher Q factors. In fact, defining $\varepsilon_i(f) = |H_i(f)|^2 - G_i^2$, we have:

$$\int_B \prod_{j=i}^{N} |H_i(f)|^2 df = \prod_{j=i}^{N} G_i^2 B + \delta_G \qquad (3.37)$$

$$\delta_G = \sum_{j=i}^{N} \underbrace{\prod_{\substack{k\epsilon(i,...,N-1) \\ k \neq j}} G_k^2 \int_B \varepsilon_j df}_{=0} + F(\varepsilon_j \varepsilon_k, ...) \qquad (3.38)$$

where first-order terms in ε_j are grouped together and are zero by definition whereas F captures higher-order terms. Filter linearity is characterized using both IIP3 as a function of frequency. Equivalently, the expression $IM3 = V_i^2/IIP3^2$ can be used to relate the maximum input signal to distortion terms. Given $IIP3_i$ constraints for each cell, the filter IIP3 can be estimated as a function of frequency with:

$$\frac{1}{IIP3^2} = \frac{1}{IIP3_1^2} + \sum_{n=2}^{N} \left(\frac{\prod_{i=1}^{n-1} |H_i(f)|^2}{IIP3_n^2} \right) \qquad (3.39)$$

since the overall frequency behavior is relevant when sizing filters for different standards and different frequency ranges. Classical assumptions are that the contributions given by the first-order and third-order Volterra kernels of each biquad sum in their absolute values (worst-case hypothesis), whereas the contributions given by the second-order Volterra kernels are supposed to be negligible, as generally the case in fully differential architectures.

A cascade level optimization problem is used to determine an optimal biquad order and assign gain to each cell. Even if from a theoretical standpoint the order of H_i in the filter $H(s)$ is irrelevant, implementation-wise it makes a big difference on the performances achievable by the filter. Based on experience and intuition, sorting H_i according to increasing pole Q appears to be a good choice leading to optimal overall linearity. On the other hand, noise considerations may indicate the opposite criterion for cascading $H_i s$ in order to increase the first stage EBG and reduce the filter input referred noise. Moreover, different gain constants assigned to each cell would differently determine the signal level, and hence the dynamic range for each biquad, even if they do not affect the global filter frequency response. Both problems of section ordering and gain assignment have been faced in the past using linear programming techniques (Halfin, 1970; Snelgrove and Sedra, 1978; Schaumann and Valkerburg, 2004) to maximize the filter dynamic range. However, increasing importance of power savings in hand-held devices suggests focusing on power optimization for a given filter type and order while guaranteeing minimum performance levels. Given the space Π of possible permutations $H_1, .., H_N$ of biquad cells we find:

$$\min_{x \epsilon \Pi} P(\pi, Z_{load}) \tag{3.40}$$

subject to

$$\begin{cases} \displaystyle\prod_{i=1}^{2} K_i = k \\ IRN_{TOT}^2 \leq (V_{min}^{max})^2 / B \\ \displaystyle\min_{f \epsilon B} IIP3(f) \geq IIP3^{min} \end{cases} \tag{3.41}$$

where k the filter gain, IRN_{TOT}^2 is the global input referred noise PSD in the filter bandwidth B, V_{min}^{max} the maximum RMS input noise in B and $IIP3_{min}$ the minimum IIP3 required. Power P is computed relying on an architecture dependent power estimator. Because of the complex mathematical expression of the constraints and their implementation dependent nature an exhaustive optimization, approach is adopted by calculating the cost function for all the possible candidate cascades. Even if $N!$ possible combinations of biquad cells exist in practice the approach is feasible leveraging available computational

resources since filters with order larger than 10 ($N = 5$) are very unusual
for cascade designs. The cascade optimization procedure can be outlined as
follows:

- Given a permutation gain constants K_i are assigned as in (Schaumann
  and Valkerburg, 2004) in order to place equal stress on all op-amps and
  process the maximum possible undistorted input signal. This step guaran-
  tees that strongly nonlinear behavior, such as op-amp slewing and saturation,
  is avoided. We therefore define:

$$A_i = \max \prod_{j=1}^{i} |h_j(j\omega)|, \tag{3.42}$$

where h_j is the normalized biquad frequency response implicitly defined in
3.33, and assign gain constants as follows:

$$\begin{cases} K_i = k\dfrac{A_N}{A_1} \\ K_i = k\dfrac{A_{i-1}}{A_i}, \qquad i = 2, ..., N. \end{cases} \tag{3.43}$$

- Noise is partitioned so that each biquad gives the same contribution to the
  input global in-band Power Spectral Density (PSD). Noise requirements
  (and hence power requirements) are then relaxed proportionally to the EBG
  chain preceding each cell, according to this formula:

$$IRN_i^2 = \frac{IRN_{TOT}^2}{N} \prod_{j=1}^{i-1} G_j^2. \tag{3.44}$$

- Partial biquad synthesis is then performed to estimate $IIP3$ of each cell.
  Global $IIP3$ is computed using (3.39) and compared with system spec-
  ifications. If $IIP3$ is in the requested range, power $P(\pi)$ is estimated
  considering noise requirements; otherwise the power budget is increased
  and synthesis repeated in the attempt of meeting linearity requirements. If
  needed power exceeds the maximum allowed the permutation is marked as
  unfeasible and the procedure is carried out again for another ordering.

3.5   Automatic Gain Control

According to the wireless standard specifications, the power of a signal received
at the antenna might vary over orders of magnitude and unwanted spectral inter-
ferers might be present right close to it. This signal should be somehow accom-
modated throughout the receiver chain so that it presents sufficient Dynamic

Range at the input of the ADC. In modern transceivers, this operation is performed by amplifiers whose gain is programmable either in discrete steps or continuously. This programmable gain is normally distributed throughout the front end according to the considerations made in paragraph 3.4.2 and it is driven by a smart algorithm that fully controls the receiver performance. This is what a Automatic Gain Control loop does. The AGC methodology generally consists of a design-time exploration and a run-time algorithm.

The *design-time exploration* involves extended cascade analysis for all the considered operational modes and corresponding environmental conditions. Based on these analyses, the design specifications are initially extracted that allow the standard compliancy. Therefore, the optimal receiver configuration in terms of filtering and gain is determined that yields to maximal quality at the ADC input. This configuration is normally stored in a look-up table. An example of optimally configured operation is visualized in Figure 3.13 where each receiver block has an operation range that is limited by noise and linearity. The signal propagating though such receiver should scale along the system to minimize the noise contribution while preserving the signal dynamic range.

In Figure 3.14, we exemplify the AGC operation versus different input power by plotting the SNAD for the WLAN standard. Different regions can be here defined: up to -55 dBm, the SNAD is entirely dominated by the noise (expressed as SNR); further up to -48 dBm, the SNAD is dominated by interferers and blockers (expressed as Signal to Out-of-Band Distortion Ratio (SDTR)); further up to -35 dBm, the SNAD is again dominated by the noise and thereafter, the distortion due to nonlinear operation (expressed as signal-to-distortion ratio or SiDR) is increasing. Anyway, Figure 3.14 shows that the SNAD is sufficiently larger than the sensitivity level over the dynamic input power range as defined in the IEEE802.11a standard for 64QAM modulation.
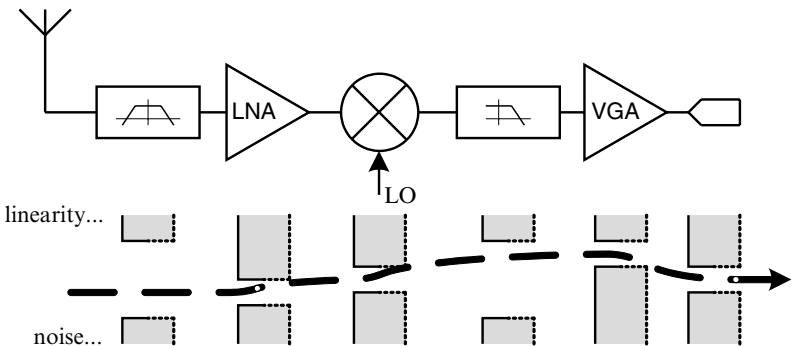
Figure 3.13.   The automatic gain control look-up table describes how to scale the signal along the receiver system.
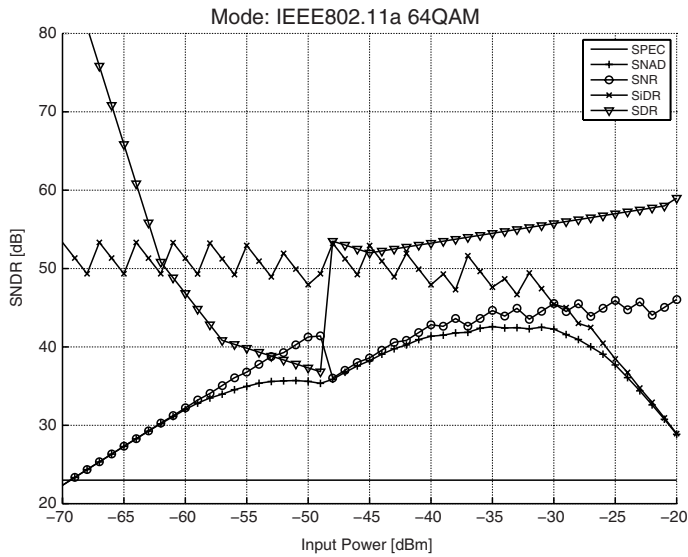
Figure 3.14.   The AGC enables sufficient signal quality to the digital receiver over a specified input power range.
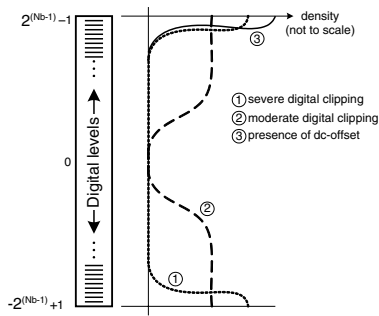
Figure 3.15.   Density functions of digital samples indicate required gain scaling.

The run-time algorithm involves detection of the input power such that the corresponding optimal receiver configuration can be applied as given in the look-up table. A power detection algorithm with rapid convergence is needed. Generally, this algorithm involves two phases, namely coarse and fine detection. During coarse detection, the gain of the receiver is scaled to avoid digital clipping: when sensing relevant signals, the receiver is configured to maximal gain and will, most likely, cause the digital received signal to be partially clipped. The density function of the digital samples roughly quantifies the source of clipping and the required gain scaling. This is shown in Figure 3.15, where three density functions are illustrated. The first density function indicates severe

Table 3.5. Analog Baseband specifications for a SDR front end.

LPF			
$f_{cut-off}$ [MHz]	Selectivity	IRN [μV_{rms}]	IIP3 [dBm]
0.1–20	$4^{\text{th}}/6^{\text{th}}$ Butterworth	80	>16
VGA			
BW [MHz]	Gain/step	IRN [$nV/\sqrt{Hz}$]	IIP3 [dBm]
$BW \gg f_c$	40 dB/3 dB	25	>20
ADC			
f_s[MHz]	♯ bits	Input range	SFDR [dBm]
10–40 MS/s	8–10	−1 dBm	20

clipping thus substantially too much gain in the receiver path. The second density function indicates moderate clipping; small gain scaling might avoid digital clipping. The third density function indicates the presence of DC offset in the receiver path that is strongly impacted by the receiver gain. During fine detection, further gain scaling might be applied considering that saturation of the analog circuits is a nonlinear process.

3.6   Conclusions

In this chapter, we discussed the specifications for an analog baseband circuit intended for a multimode direct-conversion receiver. Table 3.5 summarizes the main results for a multistandard receiver planning. The adjacent channel selectivity can be divided between analog and digital domains if the ADC have additional dynamic range: such requirements can be met in the analog domain utilizing a selective all-pole LPF. An ISI analysis has been performed exploiting the approach in Debaillie et al. (2001) and a Butterworth transfer function satisfies the BER requirements. Because of the low-input-referred noise specification, it is necessary to implement a significant amount of amplification in the RF stages otherwise the power dissipation at baseband would become pretty high. The linearity specifications can be met at baseband using suitable circuit structures.

FLEXIBLE ANALOG BUILDING BLOCKS

T HIS chapter introduces challenges and possible approaches to tackle the design of analog circuits that should provide flexible performance. The concept of Analog Design for Flexibility (ADF) is introduced that provides all the requirements to obtain a programmable analog circuit minimizing time-to-design, costs, and power consumption. Several basic analog circuit topologies, including op-amps, transconductors, and biquadratic sections are discussed and compared in terms of performance and implementation feasibility.

4.1   Challenges in Analog Design for Flexibility

As analog design is dominated by heuristics, the selection of a feasible implementation architecture comes mainly out of experience. The optimal solution is usually found only after attempting to design the circuit. Therefore, it is clear that the degree of design complexity and the time-to-design quickly outgrow when an analog circuit is required to provide a certain number of programmable features. In this case, indeed, there is not a single optimal solution but a space of solutions with a dimension proportional to the number of input specifications. The main issues to be tackled in the design of flexible analog can be grouped into four main categories:

- **Performance programmability**
  We want to cover a wide range of input specifications to make our terminal compliant with a large number of wireless standards. For each subcomponent of the transceiver, it is therefore required to provide performance programmability to maintain adequate dynamic range and accurate frequency response across the tuning range. Problems in this respect become very

acute when we are working at very high frequencies and/or the tuning range is very wide. In these situations indeed it is likely that performance programmability leads to performance degradation over the tuning range. The best implementation should come out of an accurate system-level analysis that takes the flexibility features into account since in early stages of the design and defines the most suitable design approach and topology to be used.

- **Energy scalability**
  An equally important viewpoint is the energy optimization, which allows the front end to reduce its power consumption in a particular setting when allowed by the conditions of the environment, e.g. reduce the filtering level when the interferer level is lower than the worst case defined by the standard, or defined by new users needs, e.g. moving from a WLAN to a UMTS network. This enables the SDR front end to fulfill the specifications of each standard at a power consumption similar to a single-mode radio.

- **Complexity and reliability**
  As the degree of complexity increases quickly with the required flexible features for such design, the design procedure should be as well scalable. A high number of flexible features directly influences the time of the design as well as its controllability and testability. Therefore, it is advisable to exploit modular structures replicating basic architectures in order to add the desired digital controls efficiently, making it still possible to facilitate the verification and post-layout phase for each functioning mode, minimize layout issues, and take into account the second-order effects.

- **Costs**
  Adding flexibility features may quickly lead to large chip areas. It is likely that a reconfigurable design presents higher cost in terms of silicon area compared to a single-standard circuit. The initial system level analysis should also consider eventual increasing costs due to an higher area consumption. Besides the eventual increase of the time-to-market may have an impact on the profits as well.

4.2   A Modular Design Approach

The conventional "worst case" analog design approach, in which the circuit is optimized for adequate performance while handling the most demanding tasks, is not good enough in the SDR context, as the power consumption of the analog blocks cannot be fixed but should be proportional to the the level of performance required. ADF is a design approach that takes analog performance programmability into account since the early stages of the design allowing flexibility at different levels.

Adaptive control to provide flexible frequency discrimination and gain control may currently be met with better overall performance by employing proper tunable analog circuits. A possible solution implies the use of modular circuits made of the proper combination of basic units. This indeed allows to efficiently add the desired digital controls, while minimizing layout issues. The concept of *component arrays* fits perfectly with these needs. An array is defined here as the parallel connection of dynamic analog blocks dimensioned in a binary-scaled fashion and activated whenever needed.

Figure 4.1 shows an example of ADF applied to the design of a flexible baseband filter. Given the level of flexibility needed, the optimum solution can be arrived at as:

1. The analog circuit is first finely optimized under the worst-case conditions selected within the multidimensional space of input multistandard specifications. Optimization is performed by exploiting accurate behavioral models of the analog circuits topologies which provide an optimal worst-case design, but not yet optimized for all the wanted standards.

2. Flexibility is then introduced by leveraging hardware redundancy for both active and passive components. Digital knobs are introduced in analog components making them switchable and, therefore, programmable at a software level by means of a fast digital interface. In this context, a number of recent research studies (Kangmin et al., 2006; Srinivasan et al., 2006) have demonstrated the feasibility and advantages of Network-on-Chip (NoC) over traditional bus-based architectures.
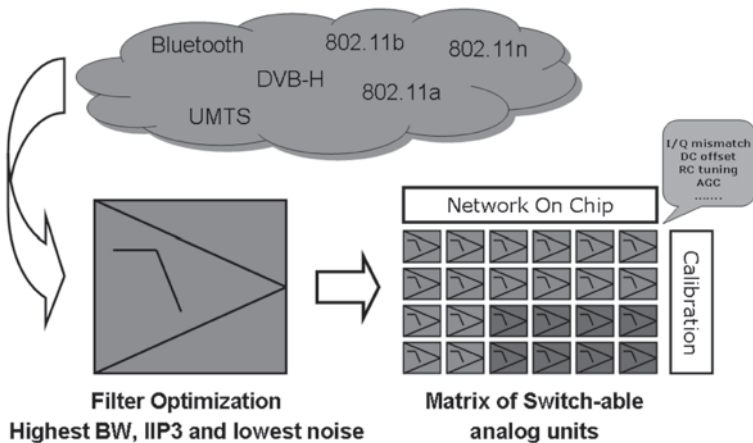
Figure 4.1. Analog design for flexibility allows to implement a high level of programmability in analog circuits.

3. Near-optimal energy/performance trade-offs are achieved by conveniently adapting the power consumption to the required performance in each functioning mode. In the envisioned cognitive radio terminal, this function will be supported by a Quality of Experience (QoE) controller which can detect the user needs and conveniently reconfigures the front end.

ADF can provide the necessary smoothness to the design process, allowing power minimization as well as a high level of controllability and testability. The idea is to use as much as possible design automation exploiting the modularity of the proposed approach.

4.3 Flexible Operational Amplifiers

The Operational Amplifier is the most important analog building block as it is part of the most common filter and amplifier topologies. A common topology for a two-stage op-amp is the Miller-compensated one (Mahattanakul and Chutichatuporn, 2005), shown in Figure 4.2. We hereby propose two possible solutions to make this op-amp topology flexible in terms of Gain-Bandwidth Product (GBW) and power consumption.

4.3.1 Variable current sources

A first example of flexible op-amp is shown in Figure 4.3 that includes a Common Mode Feedback. A fully differential Miller op-amp is made flexible by means of variable current sources and switchable input MOS transistors (D'Amico et al., 2006). The input transconductance $g_{m1,2}$ depends on the width of the input differential pair (M1–M2) as well as the current flowing in that branch, normally set by the current source transistor M5. By controlling both the current flowing through M5 and the width of M1–M2, the GBW could
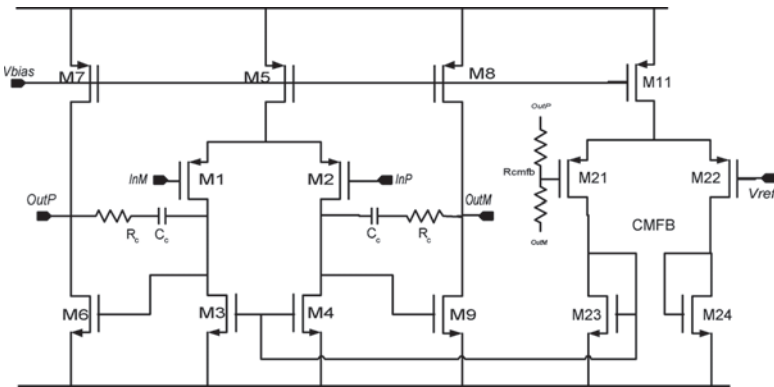
Figure 4.2. Two-stages Miller-compensated op-amp.
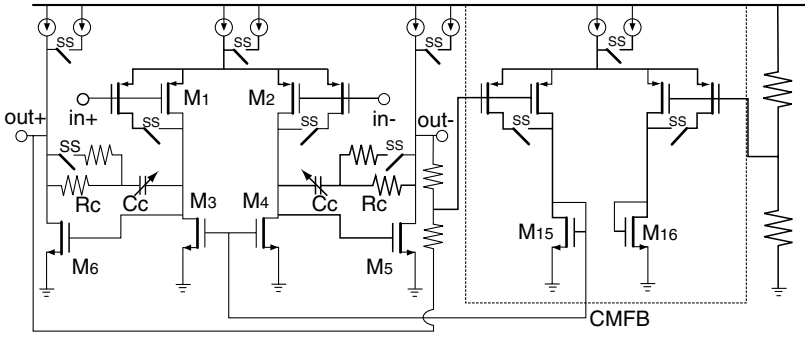
Figure 4.3. The flexible op-amp structure.

be easily modified keeping the input overdrive voltage $V_{ov1,2}$ constant. More in the detail, the transconductance $g_{m1,2}$, and therefore the GBW $= g_{m1,2}/C_C$, will linearly change with the current $I_{D1,2}$ as defined by:

$$g_{m1,2} = \frac{2I_{D1,2}}{V_{ov1,2}} \tag{4.1}$$

The second op-amp pole is determined by the output transconductance $g_{m5,6}$ and the load capacitance C_L and it is chosen so that enough phase margin is guaranteed. In case a double GBW op-amp is needed, the op-amp is first designed for the highest required GBW. By reducing the current $I_{D1,2}$ and shorting two additional transistors in parallel to the input differential pair, the GBW reduces proportionally still satisfying the stability conditions. This solution easily provides power/performance trade-offs.

4.3.2 Arrays of operational amplifiers

In case a very high level of flexibility is needed, the previous solution soon becomes not practical. An extremely flexible solution is proposed in (Giannini et al., 2006b) that exploits a Switchable Op-Amp (SOA), shown in Figure 4.4. The Switchable Op-Amp (SOA) represents the basic switchable unit of the Flexible Op-Amp (FLOA), shown in Figure 4.5, which is made up of parallel connections of SOA in a binary-scaled array. Based on the standard Miller-compensated architecture, the SOA is switched on/off through a single bit. In particular, when the op-amp is off (bit = 0), all the PMOS gates are at VDD and all the NMOS ones are grounded by means of MOS switches. Therefore, in the off mode, the op-amp shows very high output impedance and zero power consumption. The switches that carry signal must be carefully sized, trading off their finite conductance for their nonlinear characteristic. The two Miller capacitors arrays (Figure 4.5) $C_{C,array}$ are connected at the nodes C_{C1a}, C_{C1b}, C_{C2a}, and C_{C2b} while the node V_{cm} is connected to the output $OutP$ and
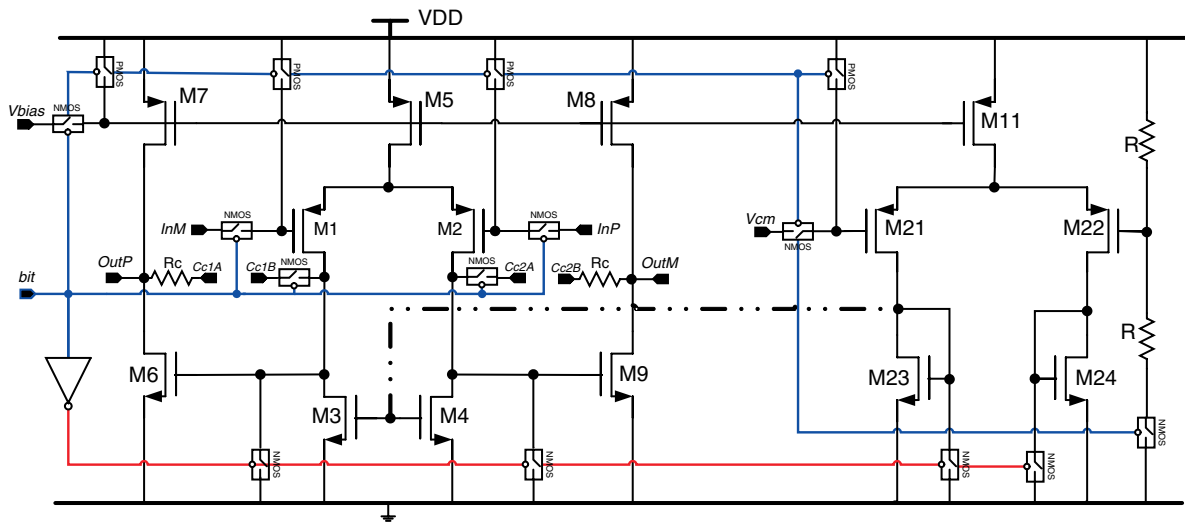
Figure 4.4. The switchable Miller op-amp (SOA) is able to null its power consumption through a single bit. All the PMOS current sources gates can be shorted at VDD through PMOS switches. The NMOS gates can be grounded by means of NMOS switches. The input PMOS transistor can be disconnected by the input pins and concurrently shorted at VDD.
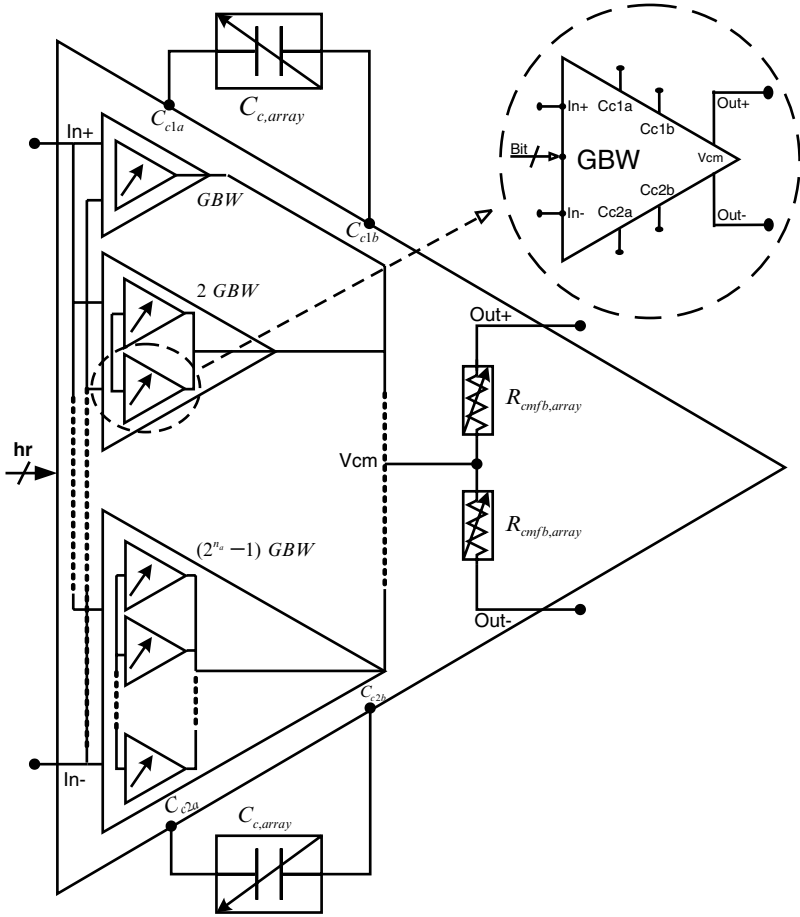
Figure 4.5. Simplified structure of the FLOA implemented as binary weighted connection of SOA (Figure 4.4). In order to minimize the silicon area, the Miller capacitor array $C_{C,array}$ and the common mode resistor arrays $R_{cmfb,array}$ are shared between all the SOA.

$OutM$ by means of two resistors R_{cmfb}. In these conditions, the poles and the zero of our SOA still maintain their original position as in a standard Miller op-amp (Mahattanakul and Chutichatuporn, 2005).

The FLOA is the basic active component of our biquadratic sections. It provides reconfigurable GBW, dynamic impedance scaling, and power scalability. The number of SOA that are switched on in a FLOA for an input digital word $\mathbf{hr} = [hr_{n_{ct}-1}, ... hr_1, hr_0]$ is given by:

$$N_{on}(\mathbf{hr}) = \sum_{k=0}^{n_{ct}-1} hr_k 2^k \tag{4.2}$$

where n_{ct} is defined in (3.28). Therefore, the FLOA unity gain frequency can be calculated as follows:

$$\omega_u(\mathbf{hr}) = \frac{g_{m1,2}}{C_C} \cdot N_{on}(\mathbf{hr}) \tag{4.3}$$

where $g_{m1,2}$ is the transconductance of the transistors M1, M2 in the op-amp input differential pair (Figure 4.4) and C_C is the dynamic Miller capacitance value set by means of the shared capacitors arrays $C_{C,array}$ in Figure 4.5. It can easily be demonstrated that the criteria to assure stability in such flexible op-amp is the same than in a standard fixed Miller op-amp (Mahattanakul and Chutichatuporn, 2005). Assuming that the nondominant pole is given by:

$$p_{nd}(\mathbf{hr}) = -\frac{\omega_{T6,9}C_C}{C_C + C_{L,tot}} \cdot N_{on}(\mathbf{hr}) \tag{4.4}$$

where $\omega_{T6,9}$ is the cut-off frequency of M6, M7 (Figure 4.4) and $C_{L,tot}$ is the sum of load capacitance C_L of the FLOA and the parasitic capacitance C_p at the output nodes. The resulting phase margin is given as:

$$\phi_M = \arctan\left(\frac{\omega_{T6,9}C_C^2}{g_{m1,2}(C_C + C_{L,tot})}\right) \tag{4.5}$$

As the number of parallel connections at the output nodes is actually proportional to the number of SOA connected in parallel, it is likely that C_p may have a high impact on the op-amp performance. A careful layout limits the parasitics and optimizes the op-amp performance. The input-referred thermal noise PSD of the FLOA is proportional to the number of active SOA and can be derived as:

$$S_n(\mathbf{hr}) = \frac{16}{3}kT\left[\frac{1}{\omega_u(\mathbf{hr})C_C}\left(1 + \frac{g_{m3,4}}{g_{m1,2}}\right)\right] \tag{4.6}$$

where $g_{m3,4}$ is the transconductance of the op-amp input stage transistors M3, M4 in Figure 4.4. This equation shows that the noise decreases as the flexible gain-bandwidth product and the Miller capacitance increase. MOS mismatches result in a nonzero offset voltage at the input of the SOA. The input offset voltage for the FLOA is just the arithmetic mean of the voltage offset reported in each single SOA currently switched. Therefore, it is given by:

$$v_{off,FLOA} = \frac{1}{N_{on}} \cdot \sum_{j=0}^{N_{on}} v_{off,SOA}(j) \tag{4.7}$$

where $v_{off,SOA}(j)$ is the mismatch induced offset of the jth SOA. Assuming that all the $v_{off,SOA}$ are equal, $v_{off,FLOA} = v_{off,SOA}$. The sensitivity of ω_u to supply voltage, process, and temperature variations can be minimized by

employing a proper bias circuit (D'Amico et al., 2006). In this circuit, the transconductance g_{m1} of transistors M1, M2 in Figure 4.4 are matched to the conductance of a internal resistor. Extensive corner simulations were performed and a maximum op-amp bandwidth variation of $\pm 3\%$ is expected. Finally, the switching time of the ω_u is dependent on several aspects (i.e. time constant switch-MOS, op-amp settling time). In case a new standard must be selected, the switching time for the FLOA and eventual transient effects related to that are not critical as sufficient time margin is available to complete this operation. On the other hand, switching time becomes critical when the op-amp has to be switched on/off to change the filter selectivity for the same standard.

4.4   A Digital-Controlled Current Follower

In Alzaher et al. (2002), a Digitally Controlled Current Follower (DCCF) and a unity gain voltage buffer was proposed. The DCCF comprises the Current Division Network (CDN) to provide digital tuning of DCCF gains (Figure 4.6). The CDN is inherently linear and can be digitally trimmed up to 10 bits without component spreading and bandwidth reduction. In addition, the R-2R ladder is incorporated into the circuit design as a programmable resistive circuit element to further increase the tuning range and allows the implementation of filters with large time constants.

4.5   Flexible Passive Components

Arrays of passive components can be used for flexible amplification and filtering. In this case, the design problem is reduced to the use of suitable switches in series with a basic passive units. These units are replicated with convenient series/parallel connections in order to create arrays of resistors and capacitors (Figure 4.7).

The capacitors arrays are the binary-weighted connection of basic units of metal interconnect capacitors. For better linearity performance, the NMOS control switches are always on the virtual ground side where the voltage swing is close to zero. The biggest nominal capacitor value C_{max} is defined by the most stringent integrated noise specification. The basic capacitor unit value is given by Corsi et al. (2007):

$$C_{basic} = \frac{C_{max}}{2^{n_{cap}} - 1} \cdot \frac{2\xi}{1 - \xi^2} \tag{4.8}$$

where n_{cap} is defined in (3.32) and ξ is the RC process deviation which is dependent on technology. For example, for $\xi = 0.4$, $n_{cap} = 7$ and $C_{max} = 30pF$ the basic capacitor $C_{basic} \simeq 225fF$. Particular care should be used in choosing a value of C_{basic} which has to be large enough not to be heavily influenced by the parasitic capacitances. This is a fundamental limitation that may constrain the flexible features (i.e. the number of bits n_{cap} and/or the maximum
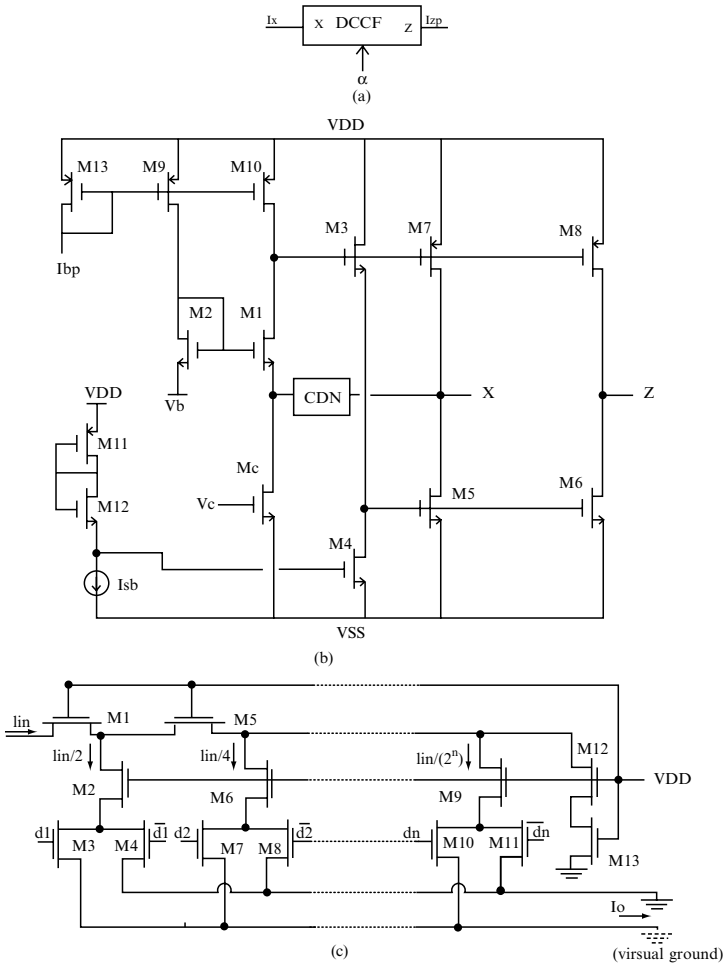
Figure 4.6. (a) DCCF symbol. (b) DCCF CMOS realization. (c) Current division network circuit diagram. (From Alzaher et al., 2002.)

noise floor). The capacitors arrays can be programmed by the digital word $\mathbf{hc} = [hc_{n_{cap}-1}, ...hc_1, hc_0]$. The resistors arrays are built as binary-weighted connection of poly-silicon resistors. The control switches are implemented as straight NMOS–PMOS Transmission Gates: this solution assures a lower ON resistance and a better linear behavior. The smallest resistor set by the resistor array is the one that allows to achieve $f_{co,max}$ with the capacitance value of C_{max}. From this assumption, the value of the basic resistor R_{basic} to be replicated is given by:

$$R_{basic} = \frac{1 - 2^{-n_{ct}}}{\pi C_{max} f_{co,max}} \quad (4.9)$$
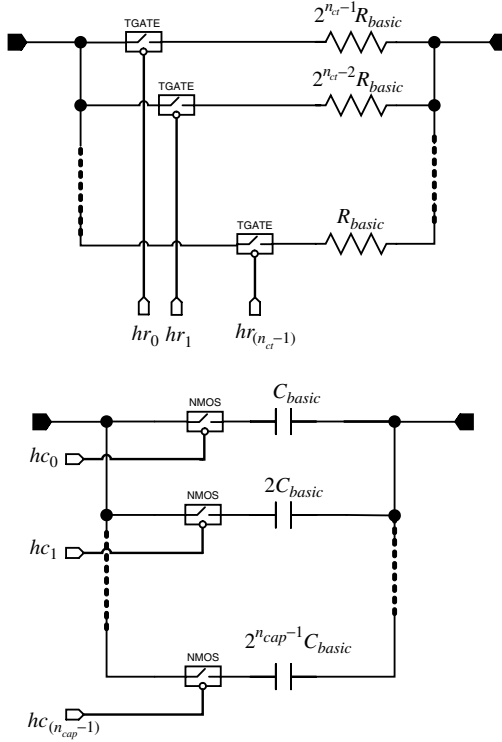
Figure 4.7. The resistors and capacitors array are the parallel connection of binary-scaled passive units. While in the resistor arrays the switches are implemented as straight transmission gates, in the capacitor arrays NMOS switches are used.

For example, if $n_{ct} = 5$, $C_{max} = 30pF$ and $f_{co,max} = 18MHz$, the basic resistor $R_{basic} \simeq 571\Omega$. (4.9) suggests another fundamental limit: once the noise floor is fixed, the maximal cut-off frequency is limited by the smallest resistor can be realized in an accurate way. The binary-scaled resistor array is implemented as a series/parallel connection of R_{basic} resistors. As the resistors arrays and the FLOA are driven by the same digital word **hr**, the resistance value of the resistor array is given by:

$$R_{array}(\mathbf{hr}) = \left(\sum_{k=0}^{n_{ct}-1} \frac{hr_k}{R_{basic}2^k} \right)^{-1} \tag{4.10}$$

4.6 Flexible Transconductors

Having a linear transconductor that can be properly tuned keeping its performance is not an easy task. If BiCMOS technology allows to design programmable transconductors taking advantage of the wide tunability of

bipolar transistors, the design in CMOS technology is much more challenging: nearly every published CMOS tunable transconductor makes use of the *linear* Pennock (1985) *or square-law* Bult and Wallinga (1987) behavior between the drain current and the gate-source voltage. Unfortunately, in such cases, the transistor characteristics deviate significantly from the ideal behavior. As very well explained in Mensink et al. (1997), this results in relatively high distortion levels in combination with a reduced transconductance tuning range. The performance of an active triode converter Pennock (1985) decreases mainly with respect to the linearity rather than the tuning range. To overcome these problems, three design strategies can be applied as proposed in Mensink et al. (1997):

1. Compensation techniques can be used in order to compensate at least for the most dominant nonlinearity. Compensation techniques are normally not robust against mismatch and usually decrease the ratio between dynamic range and power consumption. Furthermore, the cause of the most dominant nonlinearity is biasing and technology dependent. Although compensation techniques can improve the linearity, they are usually not preferable.

2. The signal voltage swing over a nonlinear device can be reduced so that a small-signal approach is valid. In this way, distortion is hardly generated and the effect of mismatch will be small. However, a small signal approach implies that the bias current is significantly larger than the signal current which can result in a noisy transconductor and a low dynamic range and power efficiency.

3. Instead of MOS transistors, linear devices can be used such as resistors. The linearity of resistors is usually sufficient and much better than that of a MOS transistor. Besides, a resistor requires no bias current. As a disadvantage, the resistance is not electrically tunable.

   Moon and Song (1993) presents a combination of techniques (such as in 2) and 3)) where a circuit containing resistors, MOS transistors, and op-amps is used. A new transconductor was developed in Mensink et al. (1997) using resistors and transistors. The transistors are used in such a way that the small-signal approach is valid as much as possible resulting in a small nonlinearity contribution. A similar approach to tune the g_m is also used in Behbahani et al. (2000); Bollati et al. (2001); Hori et al. (2003, 2004); Chamla et al. (2005).

4.7 Flexible Biquadratic Sections

There are two dominant approaches for the synthesis of CT filters. In one approach, cascades of second-order sections (called *biquads*) are used, each

section implementing a pole pair (and, if desired, a zero pair) of the transfer function. The second approach is more complicated, but can result in lower sensitivities of the pass-band frequency response to individual element values. It starts by choosing an appropriate passive LC ladder prototype (using classical analytical techniques, tables, or software), and converts it to an active circuit that does not use inductors. Almost all integrated CT filters synthesized using the above approaches contain integrators as basic building blocks. An active circuit realizing a biquadratic transfer function is called a biquad Deliyannis et al. (1999) and can be implemented with one or more op-amps. A Single Amplifier Biquadratic cell (SAB) is a biquadratic cell using one amplifier. In the flexibility perspective, a biquad should be able to easily tune its power/performances. We hereby present a biquad particularly predisposed to do that.

4.7.1 The Active-G_m-RC biquad

Active G_m-RC biquadratic cells merge advantages from both the traditional Gm-C and Active-RC approaches. In particular, since the op-amp frequency response features are themselves exploited for the overall transfer function synthesis, there is no need for op-amps with very high unity gain frequency (i.e. much larger than the filter pole frequency) and a large amount of power saving is allowed while still preserving good linearity performance. Figure 4.8 shows the second-order low-pass Active-G_m-RC cell structure in its single-ended form. A simple first-order model for the transfer function of a dominant pole-compensated op-amp, $A(s)$, is given by :

$$A(s) = \frac{A_{DC}}{1 + s/\omega_{p1}} \tag{4.11}$$

where A_{DC} is the dc gain of the op-amp and ω_{p1} is the (real-axis) dominant pole. Recall that the definition of the unity-gain frequency of an op-amp,
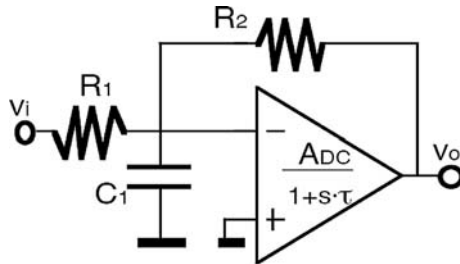
Figure 4.8. The Active-G_m-RC biquadratic cell.

ω_u, is the frequency at which $|A(j\omega_u)| = 1$. We then have the following approximation, since $\omega_u \gg \omega_{p1}$:

$$|A(j\omega_u)| = \frac{A_{DC}}{\omega_u/\omega_{p1}} = 1 \tag{4.12}$$

Thus, we have the following important equation for the first-order model:

$$\omega_u \cong A_{DC}\omega_{p1} \tag{4.13}$$

Substituting (4.13) in (4.11) for the case in which $\omega_{p1} \ll \omega \ll \omega_u$, we have at midband frequencies:

$$A(s) \cong \frac{\omega_u}{s} \tag{4.14}$$

As shown in Figure 4.9, the op-amp is assumed to present a two-stage topology. The input stage is made of the input transconductance g_{m1} and the load resistance r_{ds1}, the output stage includes the output transconductance g_{m2}, the load resistance r_{ds2}, and a Miller compensation network (the zero-nulling resistor R_C and the capacitor C_C). On the top of that, the load contribution (R_L and C_L) of the other circuits connected to the cell (as for the case of cascade higher-order filter) is shown. In Figure 4.9 an adjusting circuit sets $g_{m1} = 1/(k_G R_1)$. The adjusting circuit makes it possible to transfer the dependence of the filter frequency response on the MOS device parameters (i.e. g_{m1}) into a dependence on only the passive component values (R_1, R_2, C_1, and C_C). The low-pass filter transfer function is then given by:

$$H_{LP}(s) = \frac{\frac{1}{k_G R_1^2 C_1 C_C}}{s^2 + s\left(\frac{R_1+R_2}{C_1 R_1 R_2}\right) + \frac{1}{k_G R_1 R_2 C_1 C_C}} \tag{4.15}$$
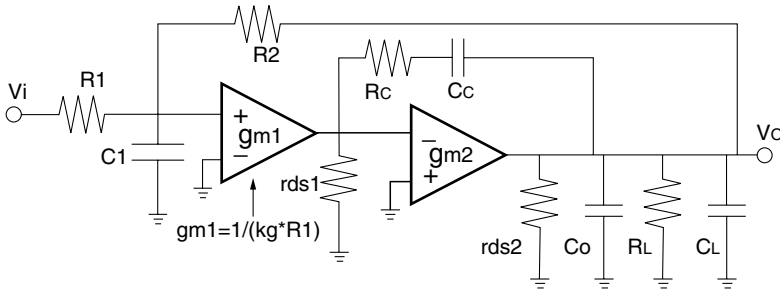
Figure 4.9.   The architecture of Active-G_m-RC cell.

The relative low-pass cell transfer function parameters (DC-gain, pole frequency, and quality factor) are:

$$
\begin{cases}
k_{LP} = \dfrac{R_2}{R_1} \\[2mm]
f_{LP} = \dfrac{1}{2\pi}\sqrt{\dfrac{1}{k_G R_1 R_2 C_1 C_C}} \\[2mm]
Q_{LP} = \dfrac{1}{1 + k_{LP}}\sqrt{\dfrac{R_2 C_1}{k_G R_1 C_C}}
\end{cases}
\tag{4.16}
$$

This Active-G_m-RC cell exhibits the following features that make it preferable for the implementation of baseband filter in portable multistandard terminals:

- **Low power consumption**
  This is a key target for portable terminals. Active-G_m-RC is a Single Amplifier Biquad and as such only one op-amp is used to synthesize a second-order transfer function, halving the power consumption compared with standard two op-amps Active-RC biquadratic cells. In addition, the op-amp frequency response is used to synthesize the filter frequency response. Thus, the op-amp unity gain bandwidth, $f_u = \omega_u/2\pi$, is comparable with the filter pole, f_{LP} (f_u/f_{LP} is lower than 2 for this design). This reduces its power consumption with respect to a standard closed-loop structure (Active-RC or MOSFET-C), in which the op-amp unity-gain bandwidth has to be much larger than the filter pole (typically $fu > 50 f_{LP}$ is used), requiring a much larger power consumption;

- **Good linearity**
  A very large linear range is achieved due to its closed-loop structure. Figure 4.13 shows the frequency response to the output node and to the op-amp input node, where the signal is always very low reducing the op-amp in-band distortion. Moreover, out-of-band signals are firstly filtered by the absolutely linear $R_1 - C_1$ low-pass filter at the input. This gives an out-of-band $IP3$ better than the in-band IP3, which is particularly interesting in telecom systems where the out-of-band linearity is crucial (and often more important than in-band linearity,) due to the higher level of out-of-band blockers.

- **Frequency response accuracy**
  The adjusting circuit makes the op-amp frequency response dependent on the passive component values (R and C) spread, which is the only spread to be compensated and this is done by the tuning system. This makes this proposal completely different from the previous works (Rao et al., 1973;

Tsukutani et al., 1996), where the op-amp frequency response is taken into account *as it is* to synthesize the desired transfer function. In this previous approach the filter transfer function strongly suffers from the op-amp frequency response sensitivity to technology, component spreading, and temperature, which is independent on the passive component spread. This is not the case of the Active-G_m-RC filters, whose frequency response is completely under the tuning system control.

4.7.1.1 Active-G_m-RC sensitivity

As the input transistor transconductance influences the overall Active-G_m-RC transfer function, it must be tuned to match the process and temperature variation of the resistors. This tuning can be achieved by using the following circuit approach, in which transistor transconductances are matched to the conductance of a resistor R_b. As a result, to a first-order effect, the transistor transconductances are independent of power-supply voltage as well as process and temperature variations. Figure 4.10 shows a feasible example of circuit structure that can be used in such cases. The current I flowing in all the branches is nearly equal thanks to the cascode current mirror, whose transistors' aspect ratios are given by:

$$\left(\frac{W}{L}\right)_{Mb3} = \left(\frac{W}{L}\right)_{Mb4} = \left(\frac{W}{L}\right)_{Mb7} = \left(\frac{W}{L}\right)_{Mb6} \qquad (4.17)$$

We may understand how we can track a transconductance to a resistor by observing the the loop consisting of the transistors $Mb1$, $Mb0$, and the resistor
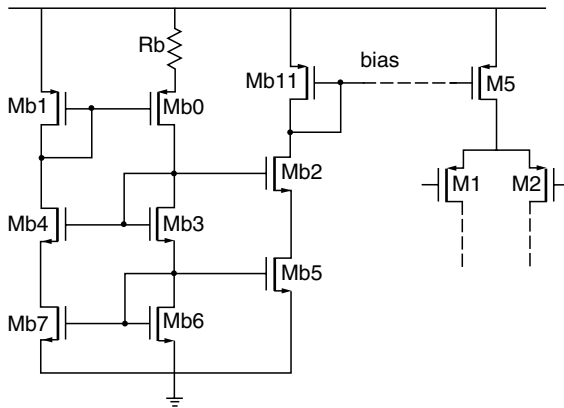
Figure 4.10. The Active-G_m-RC's bias circuit is able to track the input transconductance g_{m1} to the resistor R_b.

R_b, where the Kirchoff's Voltage Law (KVL) can be applied as follows:

$$V_{gs,Mb1} = V_{gs,Mb0} + R_b I \tag{4.18}$$

Starting from (4.18), we could easily demonstrate that the following equation is valid:

$$g_{m,Mb1} = 2 \frac{\left[1 - \sqrt{\frac{(W/L)_{Mb1}}{(W/L)_{Mb0}}}\right]}{R_b} \tag{4.19}$$

It can be shown that, based on the previous considerations, the $M1$ transconductance $g_{m,M1}$ is mainly determined by the transistors' geometric ratios, and it is independent on the power-supply voltages, process parameters, temperature, or any other parameters with large variability. In our design case, we assume $(W/L)_{Mb0} = 4 * (W/L)_{Mb1}$. Therefore, the transconductance $g_{m,Mb1}$ is matched with the input transconductance $g_{m,M1}$ through the two cascode current mirrors. We simply obtain:

$$g_{m,M1} R_b = 1 \tag{4.20}$$

Assuming (4.19) is verified, Equation (4.16) becomes:

$$\begin{cases} k_{LP} = \dfrac{R_2}{R_1} \\[2mm] f_{LP} = \dfrac{1}{2\pi} \sqrt{\dfrac{1}{R_b R_2 C_1 C_C}} \\[2mm] Q_{LP} = \dfrac{1}{1+k_{LP}} \sqrt{\dfrac{R_2 C_1}{R_b C_C}} \end{cases} \tag{4.21}$$

The bias circuit was realized and applied to the biquadratic cells. Extensive corner simulations were performed to test the overall filter performance over a temperature $(0-80°\text{C})$, process (slow–fast) and voltage supply (1.15–1.25 V) spread. A max op-amp bandwidth variation of $\pm 4\%$ is reported. The final filter frequency response presents an error due to this variation of less than 1%. It is now possible to define the sensitivity for all the parameters of the Active-G_m-RC cell as follows:

$$\begin{cases} \Gamma_{R_b}^{\omega_{LP}} = \Gamma_{R_2}^{\omega_{LP}} = \Gamma_{C_1}^{\omega_{LP}} = \Gamma_{C_C}^{\omega_{LP}} = -\dfrac{1}{2} \\[2mm] \Gamma_{R_b}^{Q_{LP}} = -\Gamma_{R_2}^{Q_{LP}} = \Gamma_{C_1}^{Q_{LP}} = -\Gamma_{C_C}^{Q_{LP}} = -\dfrac{1}{2} \\[2mm] \Gamma_{R_2}^{|H_{LP}|} = \Gamma_{C_1}^{|H_{LP}|} = \Gamma_{C_C}^{|H_{LP}|} = -\Gamma_{R_b}^{|H_{LP}|} = \dfrac{1}{2} \end{cases} \tag{4.22}$$

where we notice that the sensitivity finally does not depend on the circuit passive component values.

4.7.1.2 Active-G_m-RC noise

In order to estimate the noise contribution of an Active-G_m-RC biquad, we implement the op-amp in Figure 4.8 with the two-stage Miller-compensated topology in Figure 4.2. Assuming that only the input stage's transistors can influence the op-amp thermal noise and that we can neglect the other transistors' contribution as well as the flicker noise, the op-amp's noise PSD can be approximated to:

$$S_{oa}(\omega) \cong \frac{16kT}{3g_{m1}} \left[1 + \frac{g_{m3}}{g_{m1}} \right]$$

(4.23)

Referring to Figure 4.8, the noise performance of the overall biquadratic cell is mainly determined by the thermal noise of the resistances R_1 and R_2 and the op-amp input referred noise voltage. As the biquad PSD is given by:

$$S_{bq}(\omega) = 8kT \left[R_1 + \frac{R_1^2}{R_2} + \frac{2}{3g_{m1}} \left(1 + \frac{g_{m3}}{g_{m1}} \right) \left(1 + \frac{R_1}{R_2} \right)^2 \left(1 + \frac{Q^2}{\omega_0^2}\omega^2 \right) \right]$$

(4.24)

Figure 4.11 shows how the PSD changes with the quality factor and the k_G factor. The input referred noise integrated over the bandwidth is given by

$$IRN^2 = \frac{1}{\omega_0} \int_0^{\omega_0} S_b q(\omega)d\omega$$

(4.25)
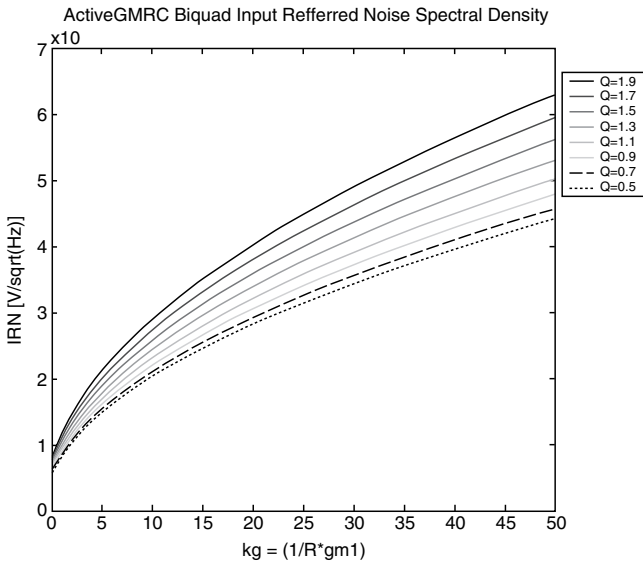
Figure 4.11. Noise spectral density of an Active-G_m-RC cell vs the k_G factor and the quality factor.

and can be calculated resulting in the following expression:

$$IRN^2 = 8kT \left[R_1 + \frac{R_1^2}{R_2} + \frac{2}{3g_{m1}} \left(1 + \frac{g_{m3}}{g_{m1}} \right) \left(1 + \frac{R_1}{R_2} \right)^2 \left(1 + \frac{Q^2}{3} \right) \right]$$

(4.26)

4.7.1.3 Active-G_m-RC Distortion

Neglecting for simplicity the distortion components due to the passive integrated components, the Active-G_m-RC nonlinearity is mainly due to its op-amp performance, i.e. the input stage transconductance nonlinearity and the output stage swing limitation. These different linearity limitations depend on the applied signal frequency, as it will be described and quantified in the following analysis. Besides, using a fully differential architecture, we also neglect the even harmonics components which do not have a significant influence on the total harmonic distortion (THD).

Input stage linearity analysis   As shown in Figure 4.12(a) and (b), for a given input signal amplitude, increasing the input signal frequency (maintaining its value lower than the filter pole frequency) corresponds to an increase of the signal amplitude at the op-amp input, because in this frequency range the op-amp open-loop gain decreases with a single pole roll-off. This increase of the input signal amplitude at the nonlinear input stage results in a nonlinear signal current, which generates distortion. When the signal frequency overcomes the filter pole frequency, the output signal amplitude decreases with the square law of the frequency due to the two-pole roll-off of the second-order frequency response and, as a consequence, the op-amp input signal decreases with a linear law.

(a) Q=1.9   (b) Q=0.5
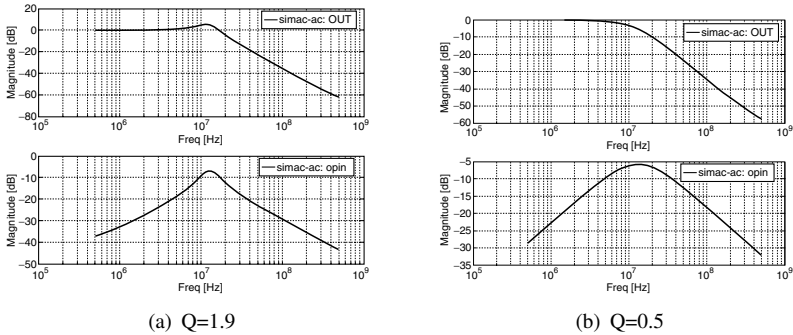
Figure 4.12.   SPECTRE simulations – AC response for the Active-G_m-RC op-amp output and the virtual ground for $Q = 1.9$ and 1.5.

(a) Input HD3   (b) Differential Pair
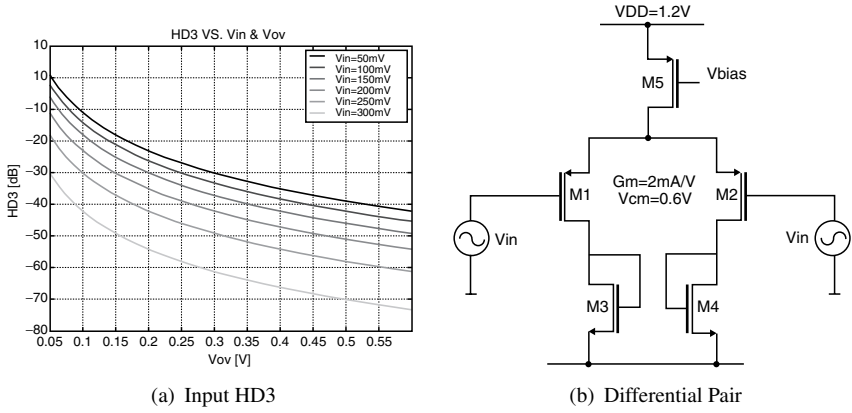
Figure 4.13. Expected input stage differential pair HD_3 vs voltage overdrive and input signal.

The Active-G_m-RC's input differential pair, shown in Figure 4.13(b), exhibits a nonlinear relationship between its differential drain current and input voltage. The contribution to the third harmonic distortion of the cell due to the input stage in open-loop configuration is:

$$HD_{3in} = \frac{V_{in}^2}{32V_{ov1}^2} \qquad (4.27)$$

where V_{ov1} is the input device overdrive voltage that is therefore the most effective parameter to control HD_{3in}. Extended SPECTRE simulations were performed to prove the validity of Equation (4.27) on deep submicron (DSP) technologies. State-of-the-art 0.13 and $0.18\mu m$ have been taken into account. The main purpose of this study was to carry out possible nonlinearity sources in the open-loop operation of the input differential pair. At the beginning, ideal tail current source and active loads were exploited.

To evaluate harmonic-distortion factor in closed-loop configuration, approach (Palumbo and Pennisi, 2003) has been exploited. Under the assumption that transistors are not driven out of their linear operating regions, small-signal analysis and conventional algebra have been used to derive the following compact expression:

$$HD_{3inCL} = \frac{V_{in}^2}{32V_{ov1}^2} \frac{|H_{LP}|^2(s)}{|A(s)|^3} |H_{LP}|(3s) \qquad (4.28)$$

We notice how $HD_{3in_{CL}}$ is frequency-dependent and increases as the frequency rises. For this reason, this limitation is important and dominates for high-frequency input signal. However, for input signal frequencies higher than

(a) HD3in vs. Vov   (b) HD3in vs. Q
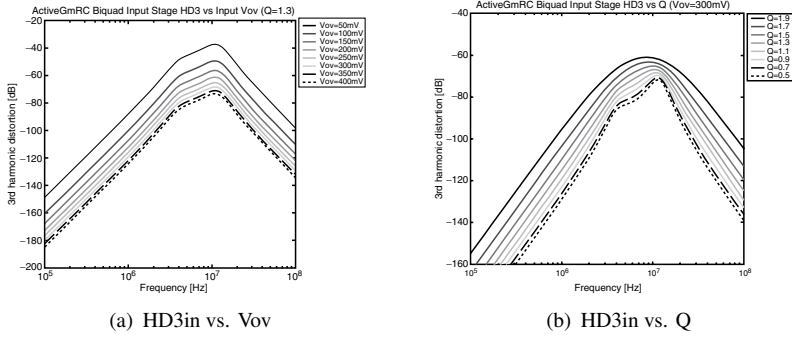
Figure 4.14. Third harmonic distortion of the input stage when V_{ov1} and Q change.

the filter pole frequency, this nonlinear behavior reduces and the filter linearity tends to increase. Figure 4.14(a) and (b) show some HD_{3inCL} simulations results.

Output stage linearity analysis At low frequencies, the op-amp gain is very large and a very small signal is present at the op-amp input nodes, since it behaves as virtual ground (Figure 4.12(a) and (b)). Therefore, the input stage exhibits a good linear behavior, and the output stage contribution to the distortion is dominant. To minimize HD_{3out}, the DC gain of the output stage A_{DCout} has to be as large as possible. In order to maximize A_{DCout}, transconductance g_{m6} of the op-amp in Figure 4.2 has to be increased by using larger width. For a given current level, the transconductance of a MOS device reaches its maximum value in the weak inversion region. In this region, a larger transistor width produces only a larger parasitic capacitances, without increasing its g_m. For this reason the output stage would have to operate at the borderline of strong and weak inversion region. In this operation region, the drain current can be written as:

$$I_{out} = I_{SS} \exp[V_{gs6}/(nV_t)] = \frac{1}{2}\mu C_{ox}\frac{W_6}{L_6}V_{ov6} \qquad (4.29)$$

where n is the slope factor, V_t is the thermal voltage, and V_{ov6} is the M6 overdrive voltage. In this way, the transconductance g_{m6} is given by:

$$\begin{cases} g_{m6} = \dfrac{I_{out}}{nV_t} \\ V_{ov6} = 2nV_t \end{cases} \qquad (4.30)$$

The exponential current relationship with V_{gs} is the main source of nonlinearity for output stage. Nonlinearities induced by other causes can be greatly suppressed by proper design. Therefore, only nonlinearities due to this cause

(a) HD3out vs. Vov   (b) HD3out vs. Q
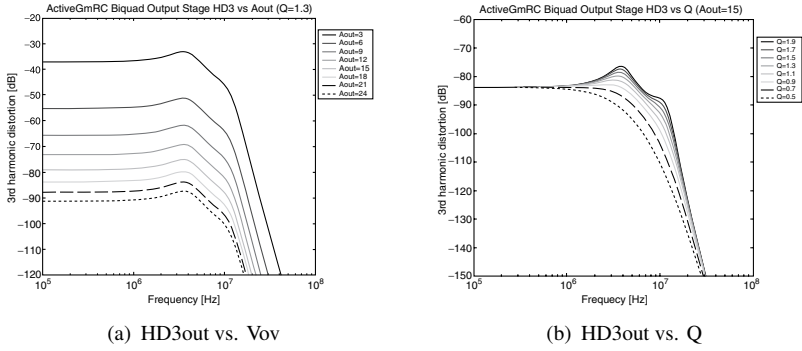
Figure 4.15.   Third harmonic distortion of the output stage when A_{DCout} and Q change.

will be investigated. Third-order harmonic distortion factor HD_{3out} for the output stage in open-loop configuration can be easily calculated as:

$$HD_{3out} = \frac{V_{in}^2}{24(nV_t)^2} \tag{4.31}$$

The third-order harmonic distortion for the output stage in closed-loop configuration HD_{3outCL} can be calculated following the same approach of HD_{3inCL} and it is given by:

$$HD_{3outCL} = \frac{V_{in}^2}{24(nV_t)^2} \frac{|H_{LP}|^2(s)}{|A(s)|^3} |H_{LP}|(3s) \tag{4.32}$$

Figure 4.15(a) and (b) shows some HD_{3outCL} simulations results.

Overall biquad linearity analysis   The linearity of the overall biquadratic section is given by the sum of the two main contributions discussed so far and it is given by the following expression:

$$HD_{3totCL} \cong HD_{3inCL} + HD_{3outCL} \tag{4.33}$$

Figure 4.16(a) and (b) shows some HD_{3totCL} simulations results.

4.7.1.4   Active-G_m-RC power consumption minimization

Given IRN and $|H(f)|$ (i.e. the DC gain K, ω_0, and Q) for each biquad, optimal synthesis is performed through a set of equations that model the SAB used as the filter core. However, any op-amp topology with a single-pole transfer function in the frequency range of interest can in principle be used. The second-stage DC gain (A_{DCout}) is set based on linearity requirements and the available supply voltage. Then, setting $M1$ and $M6$ overdrive voltages to

(a) HD3tot vs. Vov   (b) HD3tot vs. Q
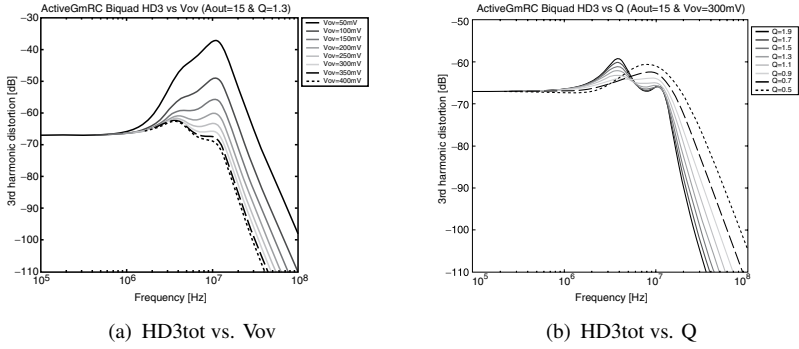
Figure 4.16. Third harmonic distortion for the Active-G_m-RC cell when V_{ov} and Q change.
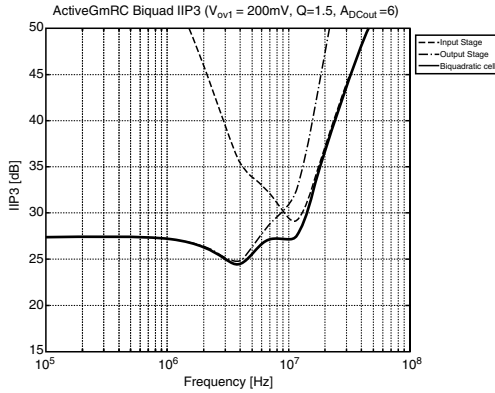
Figure 4.17. Active-G_m-RC linearity vs frequency.

initial values that provide a good trade-off with linearity, the biquad IIP3 is computed through the following equation:

$$\frac{1}{IIP3^2} = \left(\frac{3}{32V_{ov1}^2} \frac{|H(f)|^2}{|A(f)|^3} + \frac{1}{2V_{ov6}^2} \frac{|H(f)|^2}{|A_{DCout}|^3} \right) |H(3f)| \qquad (4.34)$$

where $A(f) = \omega_{GBW}/j2\pi f$ approximates the op-amp open-loop transfer function far from its dominant pole and $\omega_{GBW} = \omega_0 Q(1 + K)$. In (4.34) two contributions to overall $IIP3$ can be isolated, as shown in Figure 4.17: the first term accounts for the input stage nonlinear behavior (dominant at angular frequencies next to ω_0) whereas the second term represents the output stage contribution (dominant at lower frequencies). Equation (4.34) is computed following a simplified Volterra-based approach and the effect of the feedback loop as in Palumbo and Pennisi (2003). $IIP3$ biquad values obtained from (4.34) are used in (3.39) to compute global $IIP3$. If the filter linearity is not met, V_{ov1},

V_{ov6}, and A_{DCout} are increased and the process repeated until either linearity is met or values exceed feasible ranges. Given V_{ov1}, V_{ov6}, and A_{DCout}, the bias currents of both the input and the output stages can be computed. To simplify expressions, we define the parameter in the following equations. The biquad IRN can be expressed as a function of k_G and the input resistor R_1 through:

$$IRN^2 = 8kTR_1 \left[1 + \frac{1}{K} + \frac{8k_G}{3} \left(1 + \frac{1}{K} \right)^2 \left(1 + \frac{Q^2}{3} \right) \right] \qquad (4.35)$$

where thermal noise from resistances R_1, R_2 (set equal to KR_1) and the input stage transistors is considered. Analogously, solving (4.35) for R_1, total current I_{tot} is expressed as a function of k_G using:

$$I_{tot}(k_G) = I_{in}(k_G) + I_{out}(k_G) = \frac{V_{ov1}}{2k_G R_1(k_G)} + \frac{V_{ov6} A_{DCout}}{2R_{out}(k_G)} \qquad (4.36)$$

with $R_{out} = R_2 \parallel R_{load}$. A square law-based model is used to express bias current for $M1$ and $M6$ as a function of their overdrive voltage and transconductances g_{m1} and $g_{m6} = A_{DCout}/R_{out}$. I_{tot} has the typical dependence on k_G shown in Figure 4.18 and it is possible to find a k_{Gopt} for minimum current. Given optimal I_{tot}, R_1, and k_G, all remaining components can be determined.

C_1 and the compensation capacitance C_C are obtained matching the general biquad transfer function in (3.33) with the following expression for the Active-G_m-RC cell:

$$H(s) = \frac{\frac{1}{k_G R_1^2 C_1 C_C}}{s^2 + \left(\frac{R_1 + R_2}{C_1 R_1 R_2} \right) s + \frac{1}{k_G R_1 R_2 C_1 C_C}} \qquad (4.37)$$
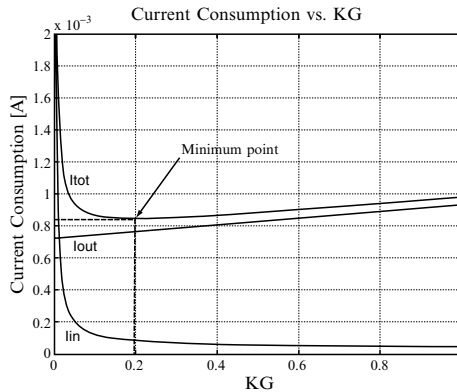
Figure 4.18.   Current consumption contributions vs kG in Active-G_m-RC cells.

Finally, MOS sizing is carried out using a model provided in the form of multidimensional tables for all transistor operating point parameters as a function of channel length and terminal voltages. In fact, since top-level performance expression are mostly based on higher-level transistor parameters (transconductance, overdrive) estimations are less sensitive to model inaccuracy. This is no longer valid during transistor sizing and MOS widths are therefore determined through interpolation of simulated data based on BSIM3 models, reaching better than 1% accuracy on the computed operating points. As for $M1$ and $M6$, their aspect ratios can be determined using relations such as:

$$\begin{cases} W_1 = g(g_{m1}, V_{ov1}, L_1) \\ W_6 = g(A_{DCout}/R_{out}, V_{ov6}, L_6) \end{cases} \tag{4.38}$$

where g denotes the tabulated function relating small signal parameters to device geometries given a fixed technology. Other op-amp devices are subsequently sized following a traditional equation-based procedure, imposing constraints on MOS saturation, phase margin, input, and output common mode. Furthermore, feasibility checks are also performed at this level to basic constraints imposed on physical parameters.

4.8 Conclusions

This chapter discussed the challenges and approaches to design analog circuits that should provide flexible performance. The concept of Analog Design for Flexibility is introduced that provides all the requirements to obtain a programmable analog circuit minimizing time-to-design, costs-and power consumption. Several basic analog circuit topologies, including op-amps, transconductors, and biquadratic sections have been analyzed in dept providing behavioral modeling for an accurate sizing.

IMPLEMENTATIONS OF FLEXIBLE FILTERS FOR SDR FRONT END

T HE motivation behind the concept of SDR, the possible solutions to make it possible integrating such a flexible radio on a single IC and its main specifications have been discussed so far. In this chapter, we firstly review the state of the art of CMOS-integrated Continuous-Time (CT) filters design from the flexibility point of view. Then, we present two silicon prototypes with whom we want to demonstrate the principles described so far in this book. We start with a dual-standard LPF for UMTS/WLAN standards with automatic integrated RC tuning circuit. Finally, we describe the implementation of a full baseband section intended for a Software Defined Radio front end.

5.1   State of the Art for Flexible CT Filters

CT filters find their application mainly in direct signal processing, especially for medium dynamic range applications, in cases where high-speed and low-power dissipation are needed. In fact, CT filters can sometimes be the only alternative since the clock feed-through problem in switched capacitor filters scales at high speeds, and digital filters can be power-hungry.

A certain level of frequency flexibility has always been present in CT filters (Durham et al., 1992). The filter frequency response is generally determined by time constants dependent on g_m,R,C that are poorly controlled in an integrated technology. The uncertainty on the nominal value of passive components due to the fabrication process can reach the $\pm 40\%$ heavily affecting the filter frequency behavior. Therefore, additional tuning circuits are usually required and a certain

degree of flexibility has to be present in order to fine-tune the cut-off frequency within a certain allowed error. In this paper, we tackle the more challenging issue to cover a wide range of cut-off frequencies with a single LPF yet maintaining the same level of accuracy. In the past, this problem was often undertaken by exploiting the G_mC topology (Mensink et al., 1997; Pavan et al., 2000; Behbahani et al., 2000; Bollati et al., 2001; Hori et al., 2003, 2004; Chamla et al., 2005). Although this topology offers power efficiency and intrinsic flexibility, it may appear poorly unless proper linearization techniques are used. Furthermore, as far as adaptive transconductors are concerned, G_mC filters may show poor robustness and performance degradation over the tuning range. An attempt to realize a flexible LPF exploiting a leapfrog architecture is reported in Hollman et al. (2001). The solution presents a low input referred noise and a good IIP3 but the power consumption is high. Furthermore, this filter presents only a few flexibility features (only WCDMA and PCM standards are supported), as a leapfrog topology does not offer many degrees of freedom. An interesting approach was also proposed in Alzaher et al. (2002) based on a digitally controlled current follower. The approach offers a good frequency tuning range, with a very high linearity and good power consumption. On the other hand, it does not provide any power scalability feature. In D'Amico et al. (2006), a UMTS/WLAN filter based on the Active G_m-RC biquadratic cells was presented that achieves a large amount of power saving while still preserving an outstanding dynamic range. Even if this solution is power efficient, still it does not achieve the degree of flexibility we need. Table 5.1 summarizes the performance of some of the most interesting designs reported in literature in the last years.

We finally realize that most of the flexible filters in literature exploit the G_mC approach, where either transconductances and/or capacitors are tuned to finely select the wanted frequency channel. Tuning g_m is ideally an easy procedure, but many second-order issues rise that irreparably degrade the performance if not properly taken into account at a design phase. If G_mC remains still the only option available for cut-off frequencies higher than 100 MHz, other approaches exist that allow to reach the same flexibility performance at lower frequencies with better linearity than the G_mC counterpart, including opamp-RC-based and mixed approaches.

5.2   A Reconfigurable UMTS/WLAN Active-G_m-RC LPF

A fourth-order low-pass continuous-time filter for a UMTS/WLAN receiver of a reconfigurable terminal is presented in this paragraph. The filter uses the cascade of two Active-G_m-RC biquadratic cells. A single op-amp is used for each biquad and its unity-gain-bandwidth is comparable to the filter cut-off

Table 5.1. Performance comparison for recent published works on Low-Pass Filters (normalized to 0 dB gain). In bold the research work of this thesis. [n.r. = not reported].

	Technique CMOS tech	Filter order	Power [mW] V/[V]	$f_{c,min}$[Hz] $f_{c,max}$[Hz]	Noise [μ Vrms]	IIP3 [dBm]
Pavan et al. (1997)	G_mC	3rd	12	2.2 M	264	17.4
	0.5 μm CMOS	Bessel	3.3	6.7 M		
Pavan et al. (2000)	G_mC	4th	70	60 M	257	n.r.
	0.25 μm CMOS	Butterworth	3.3	350 M		
Behbahani et al. (2000)	G_mC	5th	18–184	4 M	40	18.5
	0.6 μm CMOS	Elliptic	3.3	18 M	64.5	
Hollman et al. (2001)	$opampRC$	3rd, 5th	3.4, 12.7	13 k	17,47	45
	0.35 μm CMOS	Butterworth	2.7	2.1 M		
Bollati et al. (2001)	$G_mC/$	7th	57–115	30 M	n.r.	n.r.
	0.25 μm CMOS	Equiripple	2.5	120 M		
Alzaher et al. (2002)	$DCCF - RC$	6th	6.1	5 k	240	51
	0.5 μm CMOS	Butterworth	2.7	5 M	680	61
Hori et al. (2003)	G_mC	6th	10–15	1.5 M	n.r.	7.2
	0.18 μm CMOS	Elliptic	1.8	12 M		9.3
Hori et al. (2004)	G_mC	4th	1.1–4.5	0.5 M	n.r.	9.4
	0.18 μm CMOS	Butterworth	1.8	12 M		12.5
Chamla et al. (2005)	$G_mC/$	3rd	2.5–7.3	50 k	13.6	22
	0.25 μm BiCMOS	Butterworth	2.5	2.2 M	520	28
D'Amico et al. (2006)	$ActiveG_mRC$	4th	3.4–14.2	2.11 M	57	21
	0.13 μm CMOS	Bessel	1.2	11 M		
Giannini et al. (20006b)	$ActiveG_mRC$	2nd, 4th, 6th	0.7–21.6	0.35 M	78	16.7
	0.13 μm CMOS	Butterworth	1.2	23.5 M	84	19.8

frequency. Thus, the op-amp power consumption is strongly reduced w.r.t. other closed-loop filter configurations. The cut-off frequency deviation due to the technological spread, aging, and temperature variation is adjusted by an on-chip tuning circuit. The filter shares capacitors and op-amps for the two operating modes, allowing area saving with respect to the case of two separates filters, while maintaining the same linearity. Furthermore, since the two standards differ considerably in their bandwidth (2.11 and 11 MHz for UMTS and WLAN, respectively), the filter power consumption is optimized for each mode. At the same time, these cells allow satisfying the desired performance of high linearity and low noise required by the baseband filters integrated in direct conversion receivers. This filter was implemented in a $0.13\,\mu m$ Complementary Metal-Oxide-Semiconductor (CMOS) technology, occupies 0.9 mm^2, and consumes 3.4 and 14.2 mW for the UMTS and WLAN settings, respectively. It achieves a 21 dBm-IIP3 for in-band signal, while the IIP3 for out-of-band signal (blockers) increases to 31 dBm. The full chip has been designed using an automatic design tool and the experimental results agree with the expected performance.

5.2.1   Filter architecture

Figure 5.1 shows the structure of the fourth-order reconfigurable filter. This analog block is made of the cascade of two Active-G_m-RC biquadratic cells. The challenge of this design is the realization of an efficient dual-mode filter in terms of power and area occupation, operating with a supply voltage limited to 1.2 V, while guaranteeing the large linear range required by the UMTS/WLAN standards. The filter can be reconfigured in order to adjust the filter bandwidth to the selected standard (2.11 and 11 MHz for UMTS and WLAN standards, respectively), by a single Standard-Selection (SS) bit that controls the values of the resistors (this makes the overall noise proportional to kT/C for the
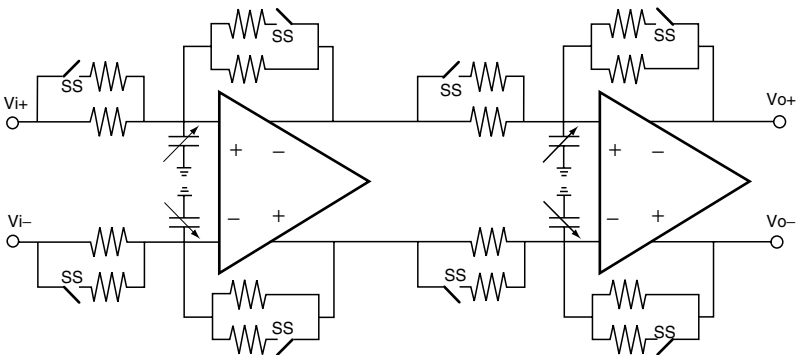
Figure 5.1.   The fourth-order reconfigurable filter structure.

Table 5.2.   UMTS and WLAN Bessel transfer function parameters.

	UMTS		WLAN	
	1st cell	2nd cell	1st cell	2nd cell
f_{LP}[MHz]	3.39	3.02	19.27	17.19
Q_{LP}	0.806	0.522	0.806	0.522
k_{LP}	1.26	1.26	1.26	1.26
f_u[MHz]	6.17	3.56	35.08	20.27
f_u/f_{LP}	1.82	1.18	1.82	1.18

two modes). In addition to that, for the UMTS case the power consumption is reduced by controlling the input stage device MOS sizes and its current levels. For both standards, the capacitors are grounded in order to be active also for the common-mode signal, otherwise a resonance at high frequency for input common-mode signals would be present. Together with the tough noise requirements, this makes the capacitance to dominate the die area. Sharing all the capacitors for the two standard configurations minimizes the area of occupation. The capacitor values are finally adjusted by the tuning circuit to compensate the technology variation. Table 5.2 summarizes the frequency response characteristics for each cell for the synthesis of a fourth-order Bessel filter transfer function.

The key feature of this structure is the use of low f_u op-amps. In fact, the ratio f_u/f_{LP} for both cells is lower than 2. This strongly reduces the op-amps power consumption. The above value has been optimized in order to minimize the power consumption using a specifically developed automatic design toolbox (Giannini et al., 2006a), which for a given specification set (noise, linearity, transfer function) directly synthesizes all the device sizes with the key target of the power minimization.

5.2.2   Automatic RC calibration scheme

Active-RC filters frequency response is determined by time constants RC that are poorly controlled in an integrated technology. The uncertainty on the passive components nominal value due to the fabrication process, temperature variations, and aging can reach the 40%, heavily affecting the filter frequency behavior. To accurately adjust the filter transfer function, additional tuning circuits are required (Tsividis, 1994; Tsividis et al., 1986; Schaumann and Tan, 1989; Tsividis and Voorman, 1993). Since the low-pass filter cut-off frequency is determined by RC products, any process variation and temperature dependencies can be compensated by tuning either the Rs or the Cs values. In this design, the tunability of the frequency response is achieved by arranging capacitive elements in digitally programmable arrays. The array value is, then,
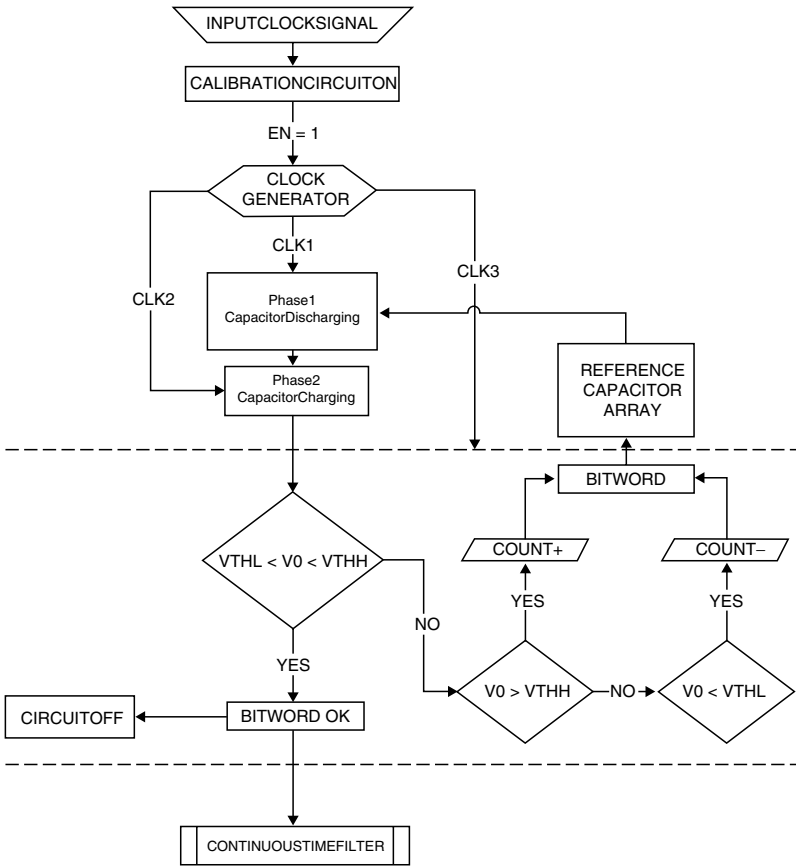
Figure 5.2.   Calibration circuit flow chart.

set using a digital code produced by an on-chip calibration circuit. Figure 5.2 summarizes in a flow chart the whole calibration circuit procedure.

The tuning scheme is based on the comparison between an isolated time constant RC and a precise external clock period. The calibration circuit requires a little amount of extra IC area. The digital code is stored in a register, therefore the calibration circuit is automatically switched off after tuning. Furthermore, the filter is insensitive either to temperature or to components variations and can be tuned in background (i.e. the filter can be used during the tuning phase). The proposed tuning scheme has been applied and debugged on a fourth-order low-pass active-RC filter, designed in a $0.13\,\mu\mathrm{m}$ CMOS technology.

Figure 5.3 shows the block diagram of the implemented on-chip calibration circuit. The circuit provides the digital word to configure the capacitors arrays in order to compensate the passive components' technological spread. The circuit requires two external input signals:

Figure 5.3. Block diagram of the calibration circuit.

1. A precise external clock signal CLK. This allows generating three different circuits clock signals thanks to a clock generator circuit implemented in the 4-bit Digital Feedback Interface. $CLK1$, $CLK2$, and $CLK3$ correspond to respective different circuit working phases.

2. An ON/OFF bit. The high-level voltage activates the output bits toward the filter arrays. The low level voltage activates the tristate output and allows forcing the arrays bits by hand.

The clock generator circuit exploits a mod4 counter and a simple logical combinatorial circuit to generate three different clock signals from the input reference one. Figure 5.4 shows the three clock signals and the three related different working phases. A resistors divider generates a DC reference voltage V_{ref}. It fixes the threshold voltages V_{THH} and V_{THL} depending on the desired frequency accuracy. Fixed nominal capacitor value C_{nom} and the time constant T_s is defined as follows:

$$T_s = \frac{1}{f_c} \qquad (5.1)$$

where f_c is cut-off frequency to be tuned. Therefore, the nominal resistor value associated to the time constant T_s results to be:
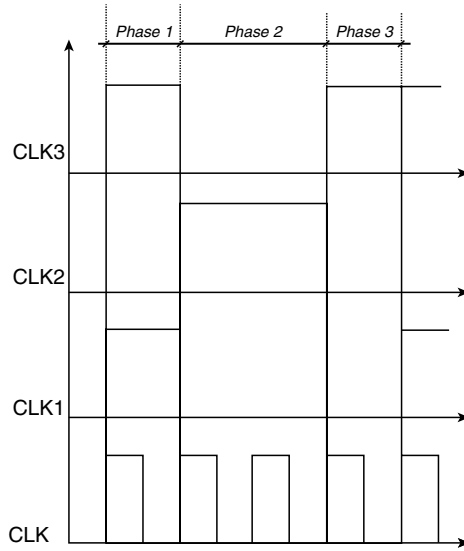
Figure 5.4.   Calibration clocks timing.

$$R_{nom} = \frac{T_s}{C_{nom}} \qquad (5.2)$$

It is now possible to calculate the current flowing in the first branch of the current cascode mirror as:

$$I = \frac{V_{ref}}{R_{nom}} \qquad (5.3)$$

The resistor series R_1, $R_1 2$, and R_3 can be conveniently sized according to the following equations:

$$\begin{cases} R_1 = R_{nom} - \dfrac{V_{THH}}{I} \\ R_2 = R_{nom} - R_1 \\ R_3 = R_2 \end{cases} \qquad (5.4)$$

During the phase 1 (ϕ_1), the MOS switches 1 and 3 (from now on $S1$ and $S3$) are on, while the MOS switch 2 (from now on $S2$) is off. This means that the capacitors array discharges because of the short circuit to the ground achieved by the $S3$. Besides, the current coming from the mirror cascode flows toward ground through the $S1$. The phase 2 (ϕ_2) requires an accurate timing as long as the right circuit working depends on it. During this phase, $S1$ and $S3$ are off. Since $S2$ is ON, the entire current coming from the cascode mirror charges the capacitors array as far as the end of the period T_s. The voltage V_0 contains the main information of the calibration circuit, i.e. it allows understanding if
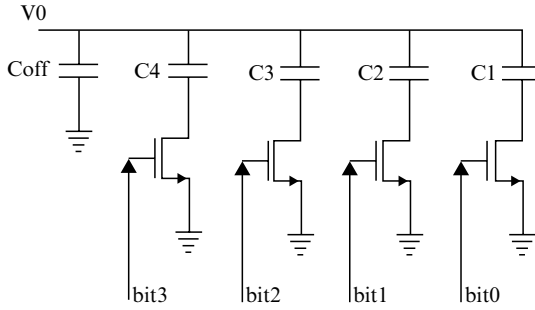
Figure 5.5. A 4 bits example of a switched capacitors array.

the given time constant corresponds to a cut-off frequency included in the range $f_c \pm 5\%$. V_0 is given by:

$$V_0 = \frac{T_s I}{C_{array}} \tag{5.5}$$

where C_{array} is the instant value of the switched capacitor array, like the one in Figure 5.5 (4 bits example.), given by the following equation:

$$C_{array} = C_{off} + \delta C \tag{5.6}$$

In the phase 3 (ϕ_3), the 4 bit Digital Feedback Interface is active. $S1$ is the only one switched on. Ideally, the charge on the capacitors array and its voltage V_0 should remain constant as far as it will be closed again either $S2$ or $S3$. V_0 is then compared with the two threshold voltages V_{THH} and V_{THL} through a simple comparator. The comparator output drives an up/down 4 bit counter. The feedback allows aligning the frequency response and, therefore, changing conveniently the capacitors array value as far as $V_{THL} < V_0 < V_{THH}$. If this condition is verified, the bits word is sent to the filter's capacitors arrays. The entire calibration circuit is switched off through an enable signal (EN) and MOS switches conveniently placed. The circuit efficiency is evaluated through MATLAB-based simulations of the passive components process deviation. Figure 5.6 shows the typical V_0 calibration procedure. The circuit works as far as $V_{THL} < V_0 < V_{THH}$. An UP/DOWN counter, that changes sequentially the digital word, makes the voltage/frequency adjustment.

Finally, Figure 5.7 shows the final results after 100 simulations comparing the initial deviated cut-off frequency and the final one. As shown, the final filter's cut-off frequency is always included in the range of allowed deviation. The tuning algorithm has been exploited in the Active-G_m-RC low-pass filter design as calibration circuit. Measurements results show a cut-off frequency accuracy within a range of $\pm 6\%$.
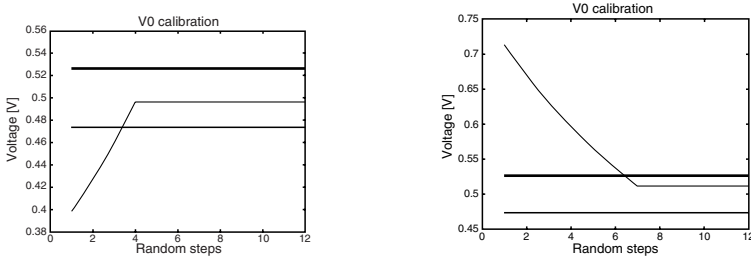
Figure 5.6. Calibration example in up/downconversion.
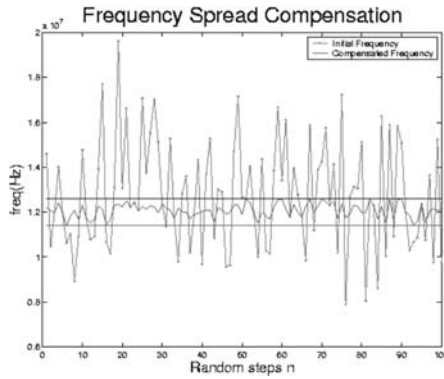
Figure 5.7. Comparison between the initial f_c and the compensated one.

5.2.3   Measurements results

The proposed fourth-order filter has been realized in a $0.13\,\mu m$ standard CMOS technology. Figure 5.8 shows the chip photograph, where the different blocks are indicated. The active area is $0.9\,\text{mm}^2$ and it is dominated by the capacitances. Therefore, the capacitance sharing for UMTS and WLAN operation modes guarantees a significant die area saving. The filter operates with a single 1.2 V supply voltage.

The several possible filter transfer functions are shown in Figure 5.9. Two nominal cut-off frequencies are possible: 2.11 MHz for UMTS and 11 MHz for WLAN, respectively. The curves in Figure 5.9 are obtained by externally changing the 4-control bits circuit. It has been verified that the tuning circuit performs a frequency step of 105.5 and 550 kHz for UMTS and WLAN, respectively.

Figure 5.10(a) shows the in-band IM3 for the UMTS setting, for two-tones (at 600 and 700 kHz) of 150 mV$_{\text{pk}}$ each. This corresponds to a $21\,\text{dBm}$ in-band IIP3 as shown in Figure 5.10(b), where also the $31\,\text{dBm}$ out-of-band IIP3 (the third harmonic falls in the filter band) is reported. Considering that the supply
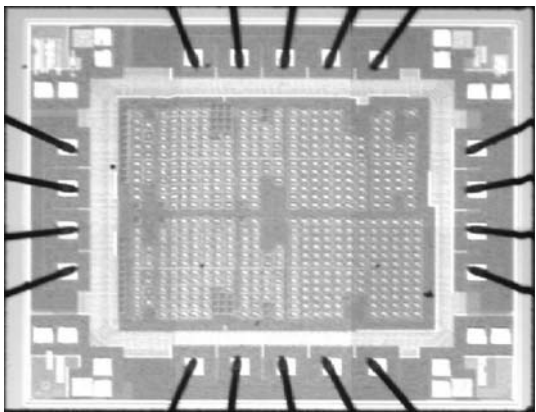
Figure 5.8. The filter chip photograph.
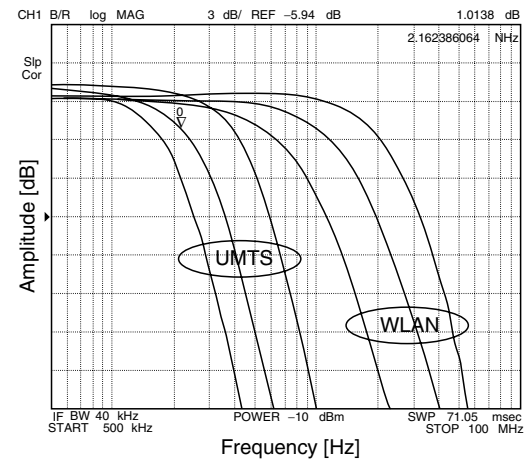
Figure 5.9. The filter transfer functions.

voltage is limited to $1.2\,\text{V}$, these results are highly performing. As expected the out-of-band IIP3 is much larger than the in-band IIP3.

On the other hand, Figure 5.11(a) shows the in-band IM3 for the WLAN setting, for two-tones at 3 and $4\,\text{MHz}$ of $178\,\text{mV}_{\text{pk}}$ each. This gives a $21\,\text{dBm}$ in-band IIP3. The IIP3 vs the central frequency of the two tones (δf is equal to $100\,\text{kHz}$ and $1\,\text{MHz}$ for UMTS and WLAN, respectively) normalized to the cut-off frequency $f_{-3\,\text{dB}}$ is shown in Figure 5.11(b). Also this graph is a demonstration of the higher IIP3 obtained for out-of-band signals.

A single tone test with $f_{in} = f_{-3\,\text{dB}}/3$ has been used to measure the THD and the $1\,\text{dBcp}$. Figure 5.12(b) shows the THD vs the input signal amplitude,
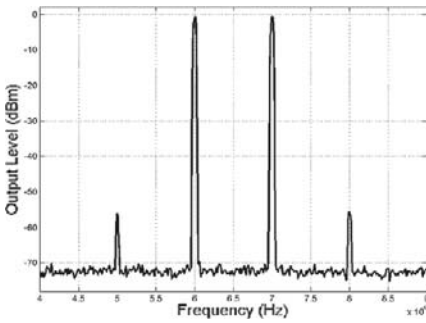
(a) IM3 - UMTS
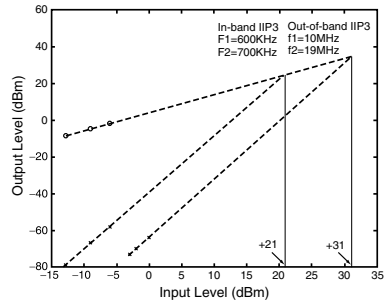
(b) IIP3 - UMTS

Figure 5.10.   The in-band IM3 and IIP3 measured for the UMTS setting.
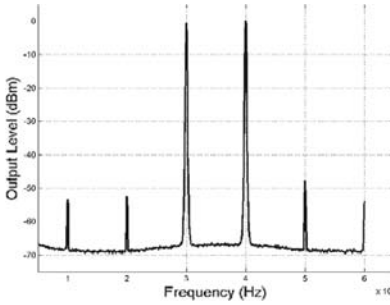
(a) IM3 - WLAN
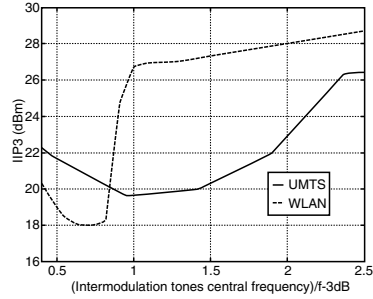
(b) IIP3 vs. Input Frequency

Figure 5.11.   The in-band IM3 for WLAN and the IIP3 measured vs input tones central frequency for the UMTS and WLAN cases.

while Figure 5.12(a) shows the 1 dBcp for both modes. For the UMTS setting, a -40 dBTHD is achieved with a 1.8 V$_{pp}$ tone amplitude, while the 1 dBcp occurs for an 11 dBm output tone amplitude (i.e. within about 70 mV from the rail). Similar performance is achieved for the WLAN setting. This demonstrates the high linearity w.r.t. the low supply voltage and low power consumption. The linearity has also been evaluated with respect the input tone frequency (f_{in}).

Since the two standards use largely different bandwidths, the current consumption of the dual-mode filter is optimized separately for each mode. It is equal to 2.9 or 11.8 mA according to the selected UMTS or WLAN standard, respectively, plus a 0.2 mA for bias. In addition the calibration circuit requires 1.8 mA. The standard selection is performed by operating on the resistors and the opamp noise is negligible. Thus, the input integrated noise is comparable for

(a) 1 dB Compression Point

(b) THD vs. Input Power
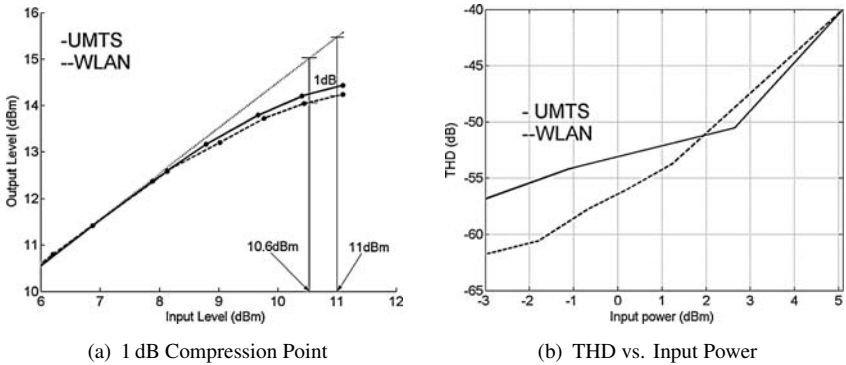
Figure 5.12. 1 dB Compression point and total harmonic distortion for both UMTS and WLAN test cases.

Table 5.3. Reconfigurable filter performance summary.

	UMTS	WLAN
Technology	0.13 μm CMOS	
Supply voltage	1.2V	
Die area occupation	0.9 mm^2	
Transfer function	4th order Bessel	4th order Bessel
f_{-3dB}	2.11 MHz	11 MHz
f_{-3dB} Programmable range	[1.45–3.6] [MHz]	[5.87–19.44] [MHz]
Max f_{-3dB} deviation	5%	
DC-gain	4 dB	4 dB
Input-referred noise	36 μVrms	36 μVrms
In-band IIP3	21 dBm	21 dBm
DR(THD = −40dB)	81 dB	81 dB
Out-of-band IIP3	31 dBm	n.a.
Power consumption	3.4 mW	14.2 mW

the two standards and it is 36 μVrms. This gives a 81 dB DR for a −40 dBTHD. Table 5.3 summarizes the filter performance.

5.3 LPF and VGA for SDR Front End

In this section, an effective solution is proposed which provides multimode operation for the baseband receiver Low-Pass Filter (LPF) and Variable Gain Amplifier (VGA) and makes them power efficient at the same time. Figure 5.13 shows a simplified block scheme of the flexible analog circuits and the digital interface. From the viewpoint of the filter functionality, channel bandwidth, noise figure, and filter selectivity are reconfigurable over a very wide range. The current consumption is proportional to the required performance. To obtain high-order filtering, we exploit a cascade of Single Amplifier Biquadratic (SAB)
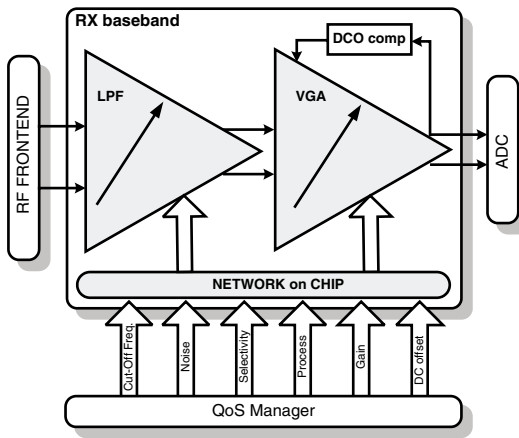
Figure 5.13. The analog baseband section is driven by a smart digital interface which fully controls its performance and power consumption by means of a fast Network on Chip. A Quality of Service (QoS) manager implements the software needed to control the digitally assisted analog circuits.

sections, namely Active-G_m-RC (D'Amico et al., 2006) and Rauch (Nichols and Rauch, 1956). This is a viable option for low-cost design since it allows power and area savings if compared with double amplifier approaches. Each SAB and the overall cascade are first finely optimized under the worst case conditions by exploiting accurate behavioral models Giannini et al. (2006a). An automatic synthesis tool is used that provides the transistor level sizing at both cell level and cascade level, guaranteeing an optimal power/perfomance trade-off and minimizing the design time. A variable gain amplifier is added to maximize the dynamic range. Finally, the overall analog baseband section is made digitally controlled and software programmable. As discussed in Section 4.1, flexibility is introduced in analog blocks by leveraging hardware redundancy for both op-amps and passive components, extending the concept of dynamic structure variation described in Tsividis et al. (2003). Near-optimal energy/performance trade-offs are achieved by conveniently adapting the power consumption to each functioning mode.

We hereby describe the final flexible baseband analog section showing that it is compliant with a wide range of wireless standards, including Bluetooth, UMTS, DVB-H, and WLAN. A silicon prototype is implemented in 0.13 μm CMOS technology with 1.2 V supply voltage which proves the feasibility and efficiency of the proposed approach. Finally, we show extensive measurements results which validate our design strategy.

5.3.1 LPF and VGA architectures

As previously mentioned, G_mC filters are more common than RC-based topolo-
gies in realizing flexible filters. However, we demonstrated that for a certain
range of input specifications, it is still more convenient to exploit op-amp-based
filter topologies that guarantee more linearity and robustness while still offer-
ing the possibility of performance scalability by exploiting the flexible analog
architectures described in Section 4.1.

Figure 5.14 shows the schematic of the flexible baseband LPF based on an
optimized cascade of Active-G_m-RC and Rauch biquadratic sections. The com-
bination of this two biquadratic cells is based on power/linearity considerations.
Active-G_m-RC cells guarantee a very good dynamic range with a limited cost
in power. However, linearity in this cell is limited by the "weak" virtual ground
of its op-amp. Therefore, the Rauch cell allows to reach the required linearity
for the overall filter. Both biquad topologies include the analog components
arrays. This solution provides this baseband block with all the required SDR
programmability.

When an Active-G_m-RC biquad uses Flexible op-amps and passive arrays
(as in Section 4.3) instead of fixed components, we obtain a fully flexible bi-
quadratic cell. Assuming unitary gain for the biquad, the design parameters for
the first fully differential Active-G_m-RC biquad shown in Figure 5.14 can be
written as:

$$
\begin{cases}
\omega_{b1}(\mathbf{hr}, \mathbf{hc}) = \dfrac{1}{2} \cdot \sqrt{\dfrac{\omega_{u1}(\mathbf{hr})}{R1 \cdot C1}} \\[4mm]
Q_{b1} = \sqrt{R1 \cdot C1 \cdot \omega_{u1}(\mathbf{hr})}
\end{cases}
\tag{5.7}
$$

where $R1$ and $C1$ are the values set respectively by $R1_{array}(\mathbf{hr})$ and $C1_{array}(\mathbf{hc})$
while $\omega_{u1}(\mathbf{hr})$ is the unity-gain bandwidth of the $FLOA_1$ defined in (4.3).
When $\omega_{u1}(\mathbf{hr})$ changes by a factor β, $R1$ changes by the inverse of this factor.
Therefore, ideally, the quality factor Q_{b1} is not dependent on the input digital
words $\mathbf{hr}$ and it is constant even when the cut-off frequency changes. On the
other hand, as ω_{u1} scales proportionally to ω_{b1}, power scalability is automat-
ically achieved in this biquadratic cell. The input referred PSD for the first
Active-G_m-RC biquad is approximately given by:

$$
S_{n,b1}(\mathbf{hr}) \cong 8kT \left[1 + R1 + \frac{8}{3\omega_{u1}(\mathbf{hr})C_{c1}} \left(1 + \frac{Q_{b1}^2}{3} \right) \right]
\tag{5.8}
$$
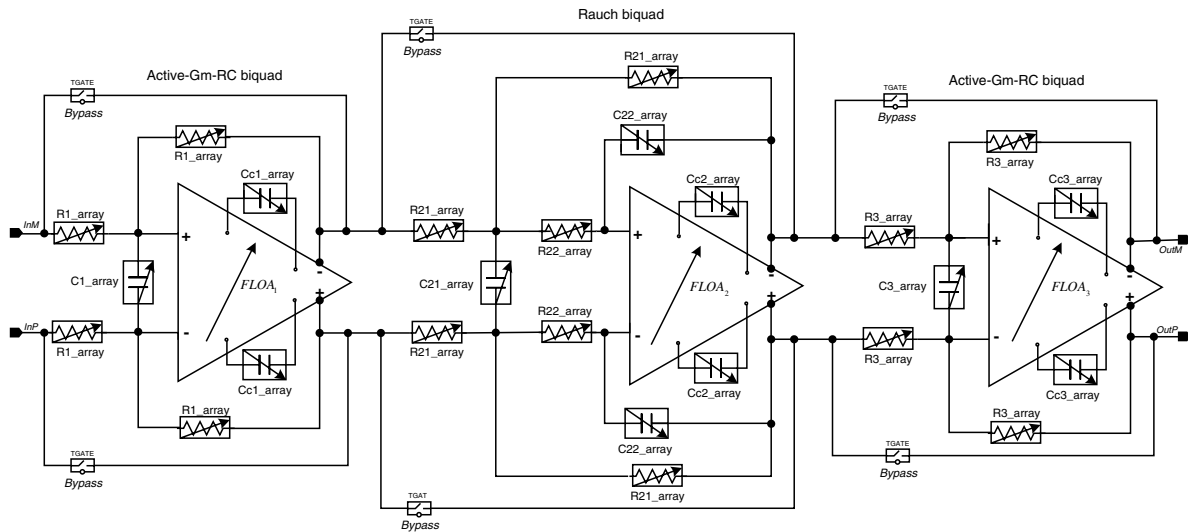
Figure 5.14. The flexible Low-Pass Filter is a combination of Active-G_m-RC and Rauch biquadratic cells. Each biquad section exploits the Flexible Op-Amp (FLOA) architecture (Figure 4.5) and the resistor and capacitor arrays (Figure 4.7). For better linearity performance, the bypass switches are implemented as straight NMOS–PMOS Transmission Gates.
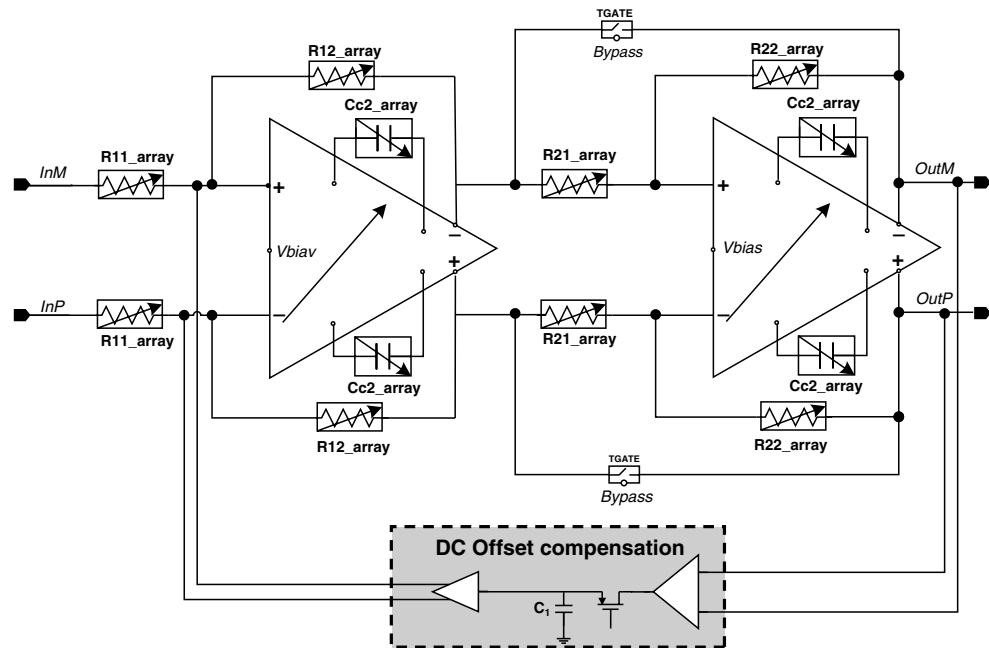
Figure 5.15. The Flexible variable gain amplifier is built from two cascaded inverting amplifiers that provide power/performance trade-offs. A simple DC offset compensation circuit senses and removes the DC-offset.

This equation shows that the PSD decreases as the cut-off frequency increases by reducing the resistor values. With a similar reasoning, assuming that its op-amp is ideal, the design parameters for a unitary gain Rauch biquadratic section in its fully differential configuration are:

$$
\begin{cases}
\omega_{b2}(\mathbf{hr}, \mathbf{hc}) = \dfrac{1}{2 \cdot \sqrt{R21 \cdot R22 \cdot C21 \cdot C22}} \\[2em]
Q_{b2} = \dfrac{1}{2 \cdot C22 \cdot (R21 + 2 \cdot R22) \cdot \omega_{b2}(\mathbf{hr}, \mathbf{hc})}
\end{cases}
\tag{5.9}
$$

where R21, R22 and C21, C22 are the values set by the correspondent arrays shown in Figure 5.14 and driven by the digital words **hr** and **hc**, respectively. Differently from the Active-G_m-RC, in the Rauch biquad the power would not scale automatically when the cut-off frequency changes. However, power scaling is obtained by driving the flexible op-amp $FLOA_2$ with the same bits **hr** of the resistors arrays R21, R22. ω_{u2} is chosen so that:

$$
\omega_{u2} = \alpha \cdot \omega_{b2} \tag{5.10}
$$

where the α factor is selected considering the effects of a finite op-amp band-width on ω_{b2} and Q_{b2} (5.9). For example, assuming to design $FLOA_2$ with a DC gain $A_{DC,2} \gg 1$ so that it has a negligible influence on the transfer function, the error made on the Rauch cell quality factor due to the finite GBW is given by:

$$
\varepsilon_{Q_{b2}} \simeq \frac{1}{1 - \frac{\alpha}{2 \cdot Q_{b2}}} \tag{5.11}
$$

where we realize that the error is minimized by choosing $\alpha \gg 2 \cdot Q_{b2}$. Design experience shows that the influence of α on the linearity performance of the Rauch cell is limited. The input referred Power Spectral Density for the Rauch biquad can be approximated as:

$$
S_{n,b2} \cong 8kT \cdot \left[R21 + 2 \cdot R22 + \frac{S_{n,FLOA2}(f)}{2kT} \right] \tag{5.12}
$$

The LPF provides the following features: coarse frequency tuning with adaptive power consumption by programming the digital word **hr**. Fine frequency tuning for RC process deviation compensation is achieved by programming the digital word **hc**. One of the power/performance trade-off we implemented is to reduce the stop-band attenuation performance in case where no large interferers or blockers signals are detected. This is accomplished by turning-off and bypassing biquadratic sections. Low on-resistance by-pass switches are implemented in each biquad. Furthermore, power consumption can be traded

for increased kT/C noise by decreasing the capacitor sizes and the transconductance and increasing the resistor values at the same time.

The VGA is built from two cascaded inverting amplifiers. The use of a FLOA makes it possible to save power by adapting the op-amp bandwidth to the expected signal bandwidth. Assuming that the open loop gain $A_{OL} \gg A_{CL}$, being A_{CL} the closed-loop (CL) gain of the FLOA, the -3 dB bandwidth for one VGA stage is approximately given by

$$\omega_{-3dB,VGA}(\mathbf{hr}) \simeq \frac{\omega_u(\mathbf{hr})}{A_{CL}} \tag{5.13}$$

In order to minimize the VGA power consumption, $\omega_{-3dB,VGA}$ should be as close as possible to the filter cut-off frequency. In this case, though, the impact of the VGA dominating poles on the baseband group delay should be also taken into account. The A_{CL} of the VGA can be modified in steps of 6 dB (First VGA stage) and 3 dB (Second VGA stage). The step can eventually be reduced by simply resizing the feedback resistor array. In our design, the impact of 3 dB more of Signal to Noise ratio has a limited impact on the receiver power budget thanks to the high efficiency of our Analog to Digital Converter (Craninckx and Van der Plas, 2007). The gain switching time is constrained by the fast Automatic Gain Control (AGC) operation and should be lower than 100 ns. In addition to that, the VGA provides different noise levels by changing the resistors arrays by fixed factors. A DC-offset compensation loop is added that senses and removes the DC-offset at power-up (in closed-loop operation) and holds the steady-state DC offset compensation value during the received burst (open-loop operation).

5.3.2 Prototype measurements

The receiver baseband section was fabricated in a 0.13 μm CMOS process with 1.2 V supply voltage. The die, shown in Figure 5.16, occupies 1.56 mm^2 for the $I-Q$ channels of both LPF and VGA. More than 60% of the overall area consumption is taken by the capacitors arrays.

Figure 5.17 shows the LPF transfer function in the 32 ($n_{ct} = 5$ bits) possible combinations of coarse cut-off frequency tuning. For a sixth-order Butterworth selectivity and 85.37 μVrms of input integrated in-band noise level, the cut-off frequency can be moved from 0.55 to 17.6 MHz with a step of 0.55 MHz. The switching time for this operation is less than 200 ns. As shown in Figure 5.18, the power consumption linearly decreases with reduced cut-off frequency: for example, the filter exhibits 13.2 mW for WLAN 802.11a (11 MHz) and 3.6 mW for UMTS 3.86 (2.11 MHz) showing lower power consumption than comparable but less flexible designs (D'Amico et al., 2006). In addition to this coarse frequency tuning, the flexible LPF provides fine frequency tuning by configuring
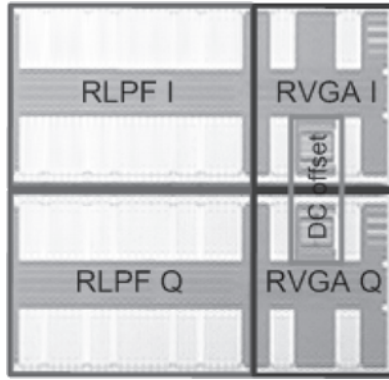
Figure 5.16.   The 0.13 µm CMOS silicon prototype takes 1.56 mm^2 for the $I-Q$ channels of both LPF and VGA.
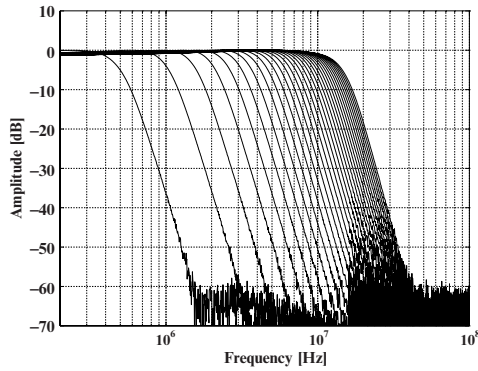
Figure 5.17.   Coarse cut-off frequency flexibility is achieved by programming the resistors arrays and the flexible Op-Amps in 32 discrete steps.
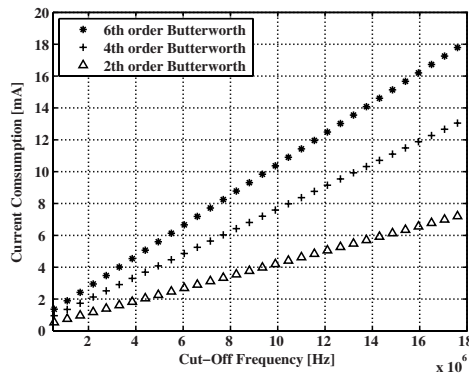
Figure 5.18.   The current consumption increases linearly with increased cut-off frequency. The filter can be made less selective by bypassing biquadratic cells while saving power at the same time. The noise level is here kept fixed at 85.35 µVrms.
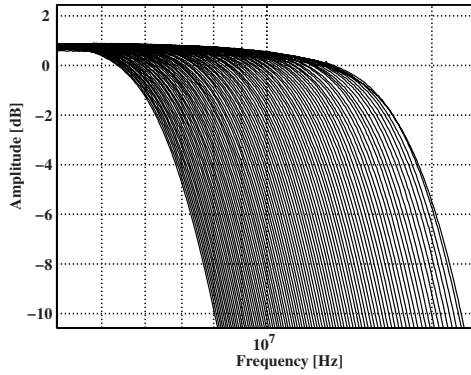
Figure 5.19. Fine cut-off frequency tuning achieved by programming the capacitor arrays. This allows to compensate the cut-off frequency for process deviation with a maximum error $\varepsilon \simeq 1.3\%$.
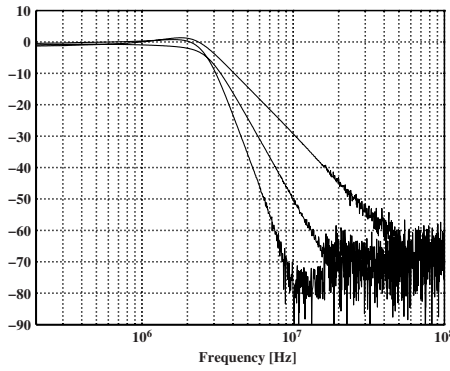
Figure 5.20. The transition band of the LPF can be changed. Second-, fourth-, and sixth-order Butterworth like selectivity are available.

its 7 bits capacitors arrays (Figure 5.19). By taking into account also this possibility, the effective frequency tuning range is included between 0.35 and 23.5 MHz. A software-based algorithm is implemented that provides accurate calibration of the cut-off frequency with a maximum error of $\pm 1.3\%$. As shown in Figure 5.20, the transition band of the filter can be traded off for less power consumption (Figure 5.18) in case no large interferers are detected or when less selectivity is required. Second-, fourth-, and sixth-order Butterworth like selectivity are available bypassing one or two biquadratic sections. Figure 5.21 shows two settings of the output noise power for the LPF set in the UMTS 3.86 standard. As shown in Figure 5.22, power consumption can be traded off for noise in case a different standard requires lower Signal to Noise ratio. When the
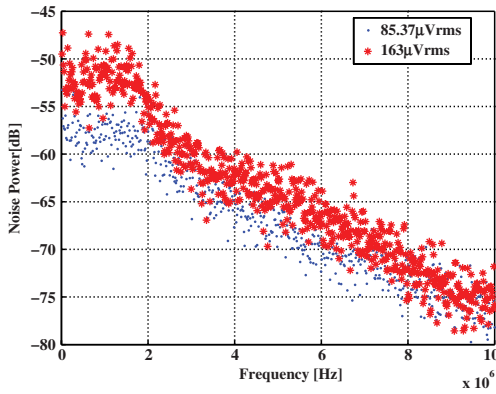
Figure 5.21.   Flexible LPF features: the noise floor of the filter can be traded off for less power consumption by conveniently configuring the capacitors arrays.
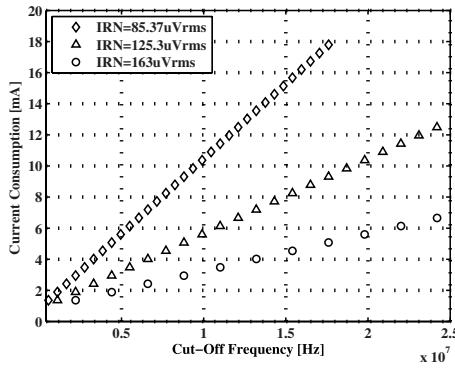
Figure 5.22.   Flexible LPF features: by modifying the integrated noise level, the current consumption and the coarse frequency step change conveniently.

noise level changes by modifying the capacitors arrays, the coarse frequency tuning step increases accordingly as shown in (3.31).

Figure 5.23 shows the IIP3 measurement at the maximum cut-off frequency available (23.5 MHz). The input tones are at 8 and 9 MHz so that the inter-modulation products are well in-band. An IIP3 of 9.96 dBVp confirms the expected result. This linearity figure of merit is nearly constant for all the cut-off frequency settings. This feature makes the proposed design a very good alternative to the less-linear G_mC filters even for flexible designs. Although, as it also happens in G_mC-based filters, the third-order intermodulation shows a certain dependance on the input tones frequency. As shown in the WLAN 802.11a measurements example of Figure 5.24, for tones close to the cut-off
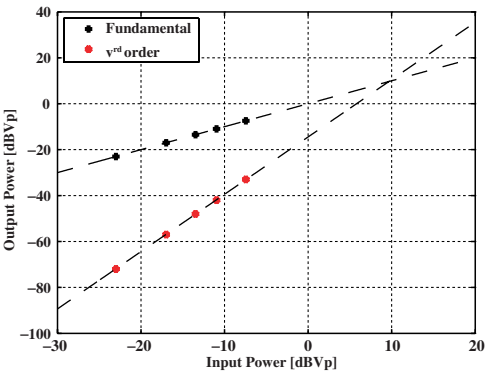
Figure 5.23. LPF linearity performance: IIP3 measurement at maximum cut-off frequency (23.5 MHz). The input tones are kept well in-band (8 and 9 MHz).
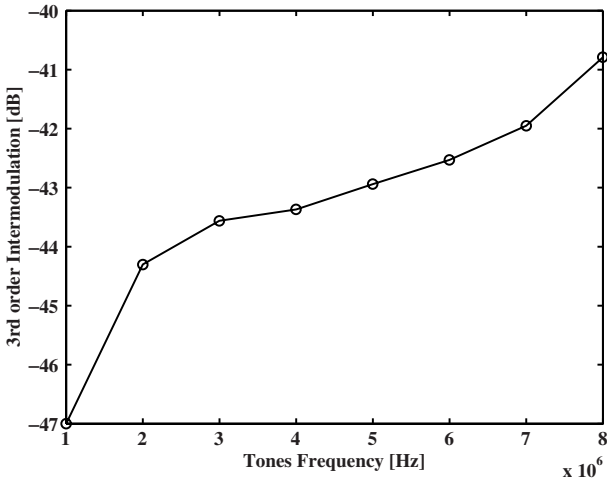
Figure 5.24. LPF linearity performance: third-order intermodulation vs average frequency between the input tones (1 MHz spacing) for the WLAN 802.11a setting. The signal amplitude for the two input tones is 106 mVpk single ended.

frequency a slight linearity worsening is present. I and Q mismatch measurements were also performed for every cut-off frequency setting. As shown in Figure 5.25, both amplitude and phase mismatch are well below the 0.25 dB and 2.8 degrees respectively. The results are not supported by any statistics as only few samples were available for measurements. Finally, Figure 5.26 shows the possible gain settings for the overall baseband section programmed in WLAN 802.11a standard. The flexible amplifier provides gain steps of 3 and 6 dB. The

(a) Amplitude I/Q mismatch   (b) Phase I/Q mismatch
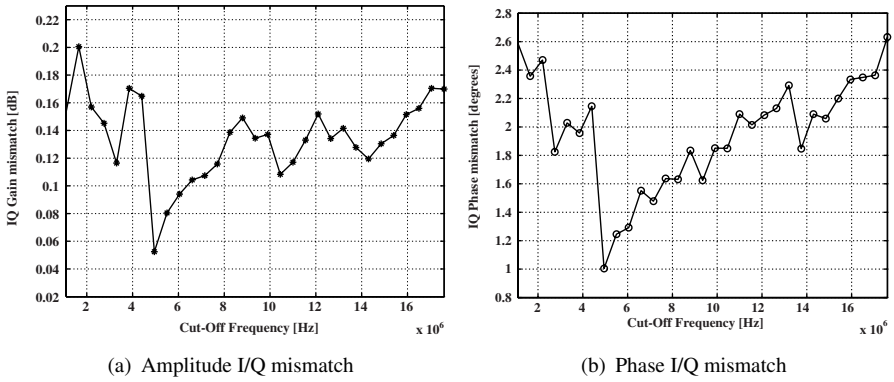
Figure 5.25.   IQ mismatch for all the cut-off frequency settings. The unbalance measurement is made at half cut-off frequency.
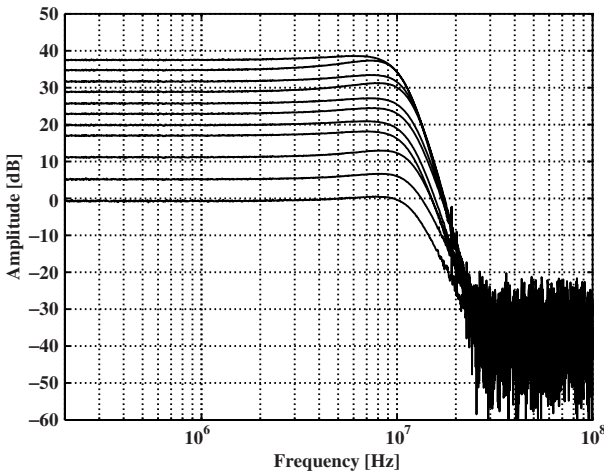
Figure 5.26.   Gain settings for LPF and VGA together in WLAN 802.11a mode. The VGA bandwidth is kept constant.

switching time is less than 100 ns so that the AGC can work properly. In order to further save power, the VGA bandwidth can be adapted to the expected signal bandwidth. Table 5.4 summarizes the main experimental results for both LPF and VGA and specifies the number of bits to control the different parameters.

For comparison with previous works, the filter performance is evaluated by the following figure of merit (Hori et al., 2004):

Table 5.4.   Performance summary.

Technology	0.13 μm CMOS	
Supply voltage	1.2 V	
Die area occupation	1.56 mm^2	
Flexible Low-Pass Filter		♯ bits
Transfer function	2th, 4th, 6th order Butterworth	3
f_{-3dB} Range	0.35–23.5 MHz	12
Max f_{-3dB} deviation	1.3%	7
DC-gain	0 dB	
Input-referred noise	85.35–163 μVrms	5+7
	[6th order – 3 power modes]	
In-band IIP3	9.96 dBV$_P$	
	[f_{-3dB}=23.5 MHz, 6th order]	
Out of band IIP3	30.34 dBV$_P$	
	[f_{-3dB}=2.11 MHz, 6th order]	
Power consumption	0.72–21.6 mW	
Flexible Variable Gain Amplifier		♯ bits
Gain range	0–39 dB	5
	3 and 6 dB steps	
f_{-3dB} range	0.18–200 MHz	24
Input-referred noise	12–40 nV/$\sqrt{\text{Hz}}$	2
In-band IIP3	>14 dBV$_P$	
Power consumption	0.36–13.5 mW	

$$FoM = \frac{P_{tot}}{N \cdot f_c \cdot SFDR \cdot N^{4/3}} \tag{5.14}$$

where P_{tot} is the total power of the filter, N is the number of poles and zeros, f_c is the cut-off frequency, $SFDR \cdot N^{4/3}$ is the normalized spurious free dynamic range, with

$$SFDR = \left(\frac{IIP3}{P_n}\right)^{2/3} \tag{5.15}$$

where $IIP3$ is the input power of the third-order intercept point and P_n is the input-referred noise power. Figure 5.27 plots the FoM for different comparable works of the last years: the present work has outstanding performance compared to less flexible designs. A slight FoM worsening is reported when we move towards low frequencies, where the flicker noise assume more influence.
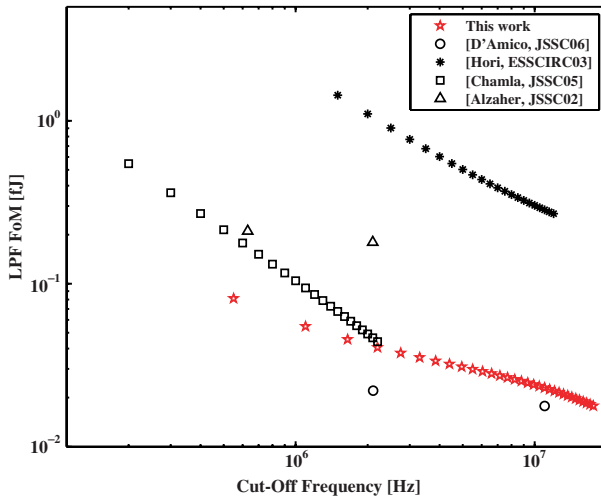
Figure 5.27.   Comparison of the presented LPF Figure of Merit with comparable flexible filters for zero-IF transceivers.

5.4   Conclusions

This chapter presented two efficient solutions to design flexible analog baseband circuits. This is demonstrated with measurements results on two prototypes. The first one is an Active-G_m-RC dual-mode (UMTS/WLAN) baseband filter for a direct-conversion receiver with an on-chip tuning system which is realized in 0.13 μm CMOS. This filter operates from a single 1.2 V supply, the required high linearity ($IIP3 > 20$ dBm) and low-noise specifications are achieved. The Active-G_m-RC biquadratic cells (with low gain-bandwidth product op-amps) minimize the power consumption. The area occupancy is minimized by sharing the capacitors. Furthermore, the power consumption is optimized for each mode.

The second example is a CMOS 130 nm implementation of a Flexible Low-Pass Filter and DC offset compensated Variable Gain Amplifier, for both of which design strategy and measurements results are detailed. A Flexible Op-Amp array provides a near-optimal power/bandwidth trade-off enabling flexibility in both filter and amplifier in terms of cut-off frequency, filter order, noise level, and gain. The prototype measurements show good agreement with the simulated performances. This complete receiver baseband section is suitable to be implemented in a Software Defined Radio Front End, where a Quality of Service Manager configures the analog blocks in the best power/performance trade-off according to the system/user/environment requirements.

Acronyms

2G Second generation

3G Third generation

4G fourth generation

ACS Adjacent Channel Selectivity

ADC Analog to Digital Converter

ADC Analog to Digital Converter

ADF Analog Design for Flexibility

AGC Automatic Gain Control

AmI Ambient Intelligence

AM Amplitude Modulated

BAN Body Area Networks

BER Bit Error Rate

BPF Bandpass Filter

BPS Band Pass Sampling

CDMA Code Division Multiple Access

CMOS Complementary Metal-Oxide-Semiconductor

CR Cognitive Radio

CT Continuous Time

DAB Digital Audio Broadcasting

DAC Digital to Analog Converter

DCCF Digitally Controlled Current Follower

DECT Digital Enhanced Cordless Telecommunications

DR Dynamic Range

DSP Digital Signal Processor

DVB-H Digital Video Broadcasting-Handhelds

EDGE Enhanced Data over GSM Evolution

EVM Error Vector Magnitude

FIR Finite-Impulse Response

FLOA FLexible Op-Amp

FoM Figure of Merit

GBW Gain-Bandwidth Product

GPRS Generalised Packet Radio Service

GPS Global Positioning System

GSM Global System for Mobile Communication

HF High Frequency

IC Integrated Circuit

ICI Inter Carrier Interference

IF Intermediate Frequency

IM3 Third-Order Intermodulation

IIP2 Input Intercept Second-Order Power

IIP3 Input Intercept Third-Order Power

IIR Infinite-Impulse Response

IP Internet Protocol

IRN Input Referred Noise

ISI Inter-Symbol Interference

LNA Low-Noise Amplifier

LO Local Oscillator

LPF Low-Pass Filter

LPS Low Pass Sampling

LSB Least Significant Bit

MAC Media Access Control

MCM-D Deposited Multi-Chip Module

MEMS Micro-Electro-Mechanical Systems

MIMO Multiple-Input Multiple-Output

NF Noise Figure

NFR Negative Frequency Rejection

NoC Network On-Chip

NoC Network on Chip

OFDM Orthogonal Frequency-Division Multiplexing

PCB Printed Circuit Board

PHY Physical Layer

PLL Phase-Locked Loop

PPA Power Pre-Amplifier

PSD Power Spectral Density

QBPS Quadrature Bandpass Sampling

QoS Quality of Service

RF Radio Frequency

RMS Root Mean Squared

SAB Single Amplifier Biquadratic cell

SDR Software Defined Radio

SDTR Signal to Out-of-Band Distortion Ratio

SFDR Spurious-Free Dynamic Range

SNR Signal to Noise Ratio

SNAD Signal to Noise and Distortion ratio

SOA Switchable Op-Amp

SR Software Radio

SSB Single-Side Band

UBPS Uniform Bandpass Sampling

UMTS Universal Mobile Telecommunications System

UWB Ultra Wide band

VCO Voltage-Controlled Oscillator

VGA Variable Gain Amplifier

WiMAX Worldwide Interoperability for Microwave Access

WLAN Wireless Local Area Network

WPAN Wireless Personal Area Network

WSN Wireless Sensors Network

List of Figures

List of Tables

References

Abidi, A.A. (1995). Direct-conversion radio transceivers for digital communications. *IEEE Journal of Solid-State circuits*, 30(12):1399–1410.

Abidi, A.A. (2007). The path to the software-defined radio receiver. *IEEE Journal of Solid-State circuits*, 42(5):954–966.

Abidi, A.A. (2006). Evolution of a software-defined radio receiver's RF front-end. In *IEEE Radio Frequency Integrated Circuits Symposium*.

Akos, D., Stockmaster, M., Tsui, J., and Caschera, J. (1999). Direct bandpass sampling of multiple distinct RF signals. In *IEEE Transactions on Communications*, 47:983–988.

Alzaher, H.A., Elwan, H.O., and Ismail, M. (2002). A CMOS highly linear Channel-Select filter for 3G multistandard integrated wireless receivers. *IEEE Journal of Solid-State circuits*, 37(1):27–37.

Bagheri, R. et al. (2006). An 800-MHz-6-GHz Software-Defined Wireless Receiver in 90-nm CMOS. *IEEE Journal of Solid-State Circuits*, 41(12): 2860–2876.

Behbahani, F., Tan, W., Karimi-Sanjaani, A., Roithmeier, A., and Abidi, A. (2000). A broad-band tunable CMOS channel-select filter for a low-if wireless receiver. *IEEE Journal of Solid-State circuits*, 35(4):476–489.

Boekhorst, F. (2002). Ambient Intelligence, the next paradigm for consumer electronics: How will it affect silicon. In *IEEE International Solid-State Circuits Conference*, San Francisco, California.

Bollati, G., Marchese, S., Demicheli, M., and Castello, R. (2001). An eighth-order CMOS Low-Pass filter with 30-120MHz tuning range and programmable boost. *IEEE Journal of Solid-State circuits*, 36(7):1056–1066.

Bose, V., Ismert, M., Welborn, M., and Guttag, J. (1999). Virtual radios. *IEEE Journal on Selected Areas in Communications*, 17(4):591–602.

Bougard, B., Pollin, S., Dejonghe, A., Catthoor, F., and Dehaene, W. (2006). Cross-layer power management in wireless networks and consequences on system-level architecture. *IEEE Signal Processing Journal*, 86:1792–1803.

Bougard, B. (2006). *Cross-Layer Energy management in broadband wireless transceivers*. Ph.D. thesis, Katholieke Universiteit Leuven.

Bult, K. and Wallinga, H. (1987). A class of analog CMOS circuits based on the square-law characteristic of an mos transistor in saturation. *IEEE Journal of Solid-State circuits*, 22:357–365.

Chamla, D., Kaiser, A., Cathelin, A., and Belot, D. (2005). A Gm-C low-pass filter for Zero-IF mobile applications with a very wide tuning range. *IEEE Journal of Solid-State circuits*, 40(7):1443–1450.

Chan, P.K. and Wilson, G. (1992). Mobility degradation effects in CMOS differential pair transconductors. *Kluwer Academic: Analog Integrated Circuits and Signal Processing*, 2:27–31.

Chehrazi, S. et al. (2005). A 6.5GHz wideband CMOS Low Noise Amplifier for multi-band use. In *IEEE Custom Integrated Circuits Conference*, pages 801–804.

Come, B. et al. (2004). Single-package direct-conversion receiver for 802.11a wireless LAN enhanced with fast converging digital compensation techniques. In *IEEE MTT-S International Microwave Symposium Digest*.

Corsi, F. et al. (2007). Tuning of high-speed telecommunication filters, via i/o cross-correlation evaluation. *IEEE Transactions on Circuits and Systems I*, 54(2):329–337.

Craninckx, J. and Donnay, S. (2003). 4G Terminals: How are we going to design them? In *IEEE Design Automation Conference*, San Diego, California.

Craninckx, J. et al. (2007). A fully reconfigurable Software-Defined Radio transceiver in $0.13\mu m$ CMOS. In *IEEE International Solid-State Circuits Conference*, San Francisco, California.

Craninckx, J. and Van der Plas, G. (2007). A 65fJ/Conversion-Step 0-to-50MS/s 0-to-0.7mW 9b charge-sharing SAR ADC in 90nm digital CMOS. In *IEEE International Solid-State Circuits Conference*, San Francisco, California.

D'Amico, S., Giannini, V., and Baschirotto, A. (2006). A 4th-order Active-Gm-RC reconfigurable (UMTS/WLAN) filter. *IEEE Journal of Solid-State circuits*, 41(7):1630–1637.

Davies, N.C. (2000). A high performance HF software radio. In *Eighth International Conference on HF Radio Systems and Techniques*.

De Man, H. (2005). Ambient Intelligence: Gigascale dreams and nanoscale realities. In *IEEE International Solid-State Circuits Conference*, San Francisco, California.

Debaillie, B. (2007). Calibration method for non-ideal transceivers. Patent Filed.

Debaillie, B., Come, B., Eberle, W., Donnay, S., and Engels, M. (2001). Impact of front-end filters on bit error rate performances in WLAN-OFDM transceivers. In *IEEE Radio and Wireless COnference*, pages 193–196.

Dejonghe, A., Bougard, B., Pollin, S., Craninckx, J., Bourdoux, A., der Perre, L. Van, and Catthoor, F. (2007). Reconfigurable radio sytems. *IEEE Signal Processing Magazine*.

Deliyannis, T.L. et al. (1999). *Continuous-Time Active Filter Design*. CRC Press Bocaraton, FL.

Driessche, J. Van (2005). Baseband architecture considerations for a software defined radio front-end. Technical report, IMEC.

Durham, A.M., Hughes, J.B., and Redman-White, W. (1992). Circuit architectures for high linearity monolithic continuous-time filtering. *IEEE Transactions On Circuits And Systems-II: Analog And Digital Signal Processing*, 39(9):651–657.

Giannini, V. et al. (2006a). A synthesis tool for efficient base-band filter design. In *IEEE Design Automation and Test European (DATE) conference*, Munich, Germany.

Giannini, V. et al. (2006b). Flexible baseband low-pass filter and variable gain amplifier for software defined radio front end. In *IEEE European Solid-State Circuits Conference*.

Halfin, S. (1970). Simultaneous determination of ordering and amplifications of cascaded subsystems. *Journal Optimization Theory Applications*, 6: 356–360.

Harrie A.C, Tilmans, De Raedt, W., and Beyne, E. (2003). MEMS for wireless communications: from RF-MEMS components to RF-MEMS-SiP. *IEEE Journal of Micromechanics and Microengineering*, 13:139–163.

Haspeslagh, D. et al. (1992). BBTRX: a baseband transceiver for a zero IF GSM hand portable station. In *IEEE Custom Integrated Circuits Conference*.

Hauspie, D. et al. (2006). Wideband VCO with simultaneous switching of frequency band, active core and varactor size. In *IEEE European Solid-State Circuits Conference*.

Hollman, T., Lindfors, S., Lansirinne, M., Jussila, J., and Halonen, K. (2001). A 2.7V CMOS dual-mode baseband filter for PDC and WCDMA. *IEEE Journal of Solid-State circuits*, 36(7):1148–1153.

Hori, S. et al. (2003). A widely tunable CMOS Gm-C filter with a negative source degeneration resistor transconductor. In *IEEE European Solid-State Circuits Conference*.

Hori, S. et al. (2004). Low-power widely tunable Gm-C filter with an adaptive DC-blocking, triode-biased MOSFET transconductor. In *IEEE European Solid-State Circuits Conference*.

Hui, S.Y. and Yeung, K.H. (2003). Challenges in the migration to 4G mobile systems. *IEEE Communications Magazine*.

Ingels, M. et al. (2007). A CMOS 100MHz to 6GHz Software-Defined Radio analog front-end with integrated Pre-Power Amplifier. In *IEEE European Solid-State Circuits Conference*.

Innocent, M. (2004). *Use and modeling of MEMS variable capacitors for multi-GHz radio applications*. Ph.D. thesis, Katholieke Universiteit Leuven.

Jakonis, D., Folkesson, K., Dabrowski, J., Eriksson, P., and Svensson, C. (2005). A 2.4-GHz RF sampling receiver front-end in 0.18μm CMOS. *IEEE Journal of Solid-State circuits*, 40(6):1265–1277.

Jondral, F.K. (1999). Software Defined Radio - Basics and evolution to Cognitive Radio. *Electronics - Communication Engineering Journal*.

Jussila, J. and Halonen, K. (2004). Minimization of power dissipation of analog channel-select filter and Nyquist-rate A/D converter in UTRA/FDD. In *International Symposyum on CIrcuits and Systems*.

Jussila, J. (2003). *Analog Baseband Circuits for WCDMA Direct-Conversion Receivers*. Ph.D. thesis, Helsinki University of Technology.

Kangmin, L. et al. (2006). Low-power network-on-chip for high-performance soc design. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 14(2):148–160.

Karvonen, S., Riley, T., and Kostamovaara, J. (2005). A CMOS quadrature charge-domain sampling circuit with 66dB SFDR up to 100MHz. *IEEE Transactions on Circuits and Systems I*, 52(2):292–304.

Karvonen, S., Riley, T., and Kostamovaara, J. (2006). A quadrature charge-domain sampler with embedded FIR and IIR filtering functions. *IEEE Journal of Solid-State circuits*, 41(2):507–515.

Krishnapura, N. and Tsividis, Y.P. (2001). Noise and power reduction in filters through the use of adjustable biasing. *IEEE Journal of Solid-State circuits*, 36(12):1912–1920.

Lackey, R.I. and Upmal, D.W. (1995). Speakeasy: the military software radio. *IEEE Communications Magazine*, 33(5):56–61.

Liscidini, A., Brandolini, M., Sanzogni, D., and Castello, R. (2006). A 0.13 μm CMOS front-end, for DCS1800/UMTS/802.11b-g with multiband positive feedback Low-Noise amplifier. In *IEEE Journal of Solid-State Circuits*.

Liu, M., Craninckx, J., et al. (2007). MEMS-enabled dual-band 1.8 and 5–6GHz receiver RF Front-end. In *IEEE Radio Wireless Symposium (RWS)*.

Mahattanakul, J. and Chutichatuporn, J. (2005). Design procedure for two-stage CMOS opamp with flexible noise-power balancing scheme. *IEEE Transactions On Circuits And Systems I*, 52(8):1508–1514.

Maloberti, F. (2007). *Data Converters*. Springer Dordrecht, The Netherlands.

Mastretta, D. and Svelto, F. (2002). Analysis and optimization of IIP2 in CMOS direct down-converters. In *Custom Integrated Circuits Conference*, pages 243–246.

Mensink C.H.J., and Nauta, B., and Wallinga, H. (1997). A CMOS Soft-Switched transconductor and its application in gain control and filters. *IEEE Journal of Solid-State circuits*, 32(7):989–998.

Mitola, J. (1995). The Software Radio architecture. *IEEE Communications Magazine*.

Mitola, J. (1999). Software Radio architecture: a mathematical perspective. *IEEE Journal on selected areas in communications*, 17(4):514–538.

Moon, U.K. and Song, B.S. (1993). Design of a low-distortion 22-khz $5th$ order Bessel filter. *IEEE Journal of Solid-State circuits*, 28:1254–1264.

Muhammad, K. et al. (2006). The first fully integrated Quad-Band GSM/GPRS receiver in a 90-nm digital CMOS process. *IEEE Journal of Solid-State Circuits*, 41(8):1772–1783.

Muller-Weinfurtner, S.H. (1999). Frequency-domain frame synchronization for optimum frequency-differential demodulation of odfm. In *Global Telecommunications Conference*.

Nguyen, C.T.-C. (2006). Integrated micromechanical circuits for RF front ends. In *IEEE European Solid-State Circuits Conference*.

Nichols, M.H. and Rauch, L. (1956). *Radio Telemetry*. Wiley, New York.

Ozgun, M.T., Tsividis, Y.P., and Burra, G. (2006). Dynamic power optimization of active filters with application to zero-IF receivers. *IEEE Journal of Solid-State circuits*, 41(6):1344–1352.

Palaskas, Y., Tsividis, Y.P., Prodanov, V., and Boccuzzi, V. (2004). A "Divide and Conquer" technique for implementing wide dynamic range Continuous-Time filters. *IEEE Journal of Solid-State circuits*, 39(2):297–307.

Palumbo, G. and Pennisi, S. (2003). High-frequency harmonic distortion in feedback amplifiers: Analysis and applications. *IEEE Transactions On Circuits And Systems I*, 50(3).

Pavan, S., Tsividis, Y.P., and Nagaraj, K. (2000). Widely programmable high-frequency Continuous-Time filters in digital CMOS Technology. *IEEE Journal of Solid-State circuits*, 35(4):503–511.

Pennock, J.L. (1985). CMOS triode transconductor for continuous-time active integrated filters. *IEEE Electronics Letters*, 21(18):817–818.

Pollet, T. and Peeters, M. (1999). Synchronization with dmt modulation. *IEEE Communications Magazine*, 37:80–86.

Rao, K.R. et al. (1973). A bandpass filter using the operational amplifier pole. *IEEE Journal of Solid-State circuits*, 8(3):245–246.

Razavi, B. (1999). CMOS RF receiver design for wireless LAN applications. In *IEEE Radio and Wireless Conference*.

Razavi, B. (1998). *RF Microelectronics*. Prentice Hall PTR New Jersey.

Rubenstein, R. (2007). Radios get smart. *IEEE Spectrum*.

Schaumann, R. and Tan, M.A. (1989). The problem of on-chip automatic tuning in continuous-time integrated filters. In *Proc. International Symposium on Circuits and Systems*.

Schaumann, R. and Van Valkerburg, E. (2004). *Design of Analog Filters*. Oxford University Press Oxford.

Schuchert, A., Hasholzner, R., and Antoine, P. (2001). A novel IQ imbalance compensation scheme for the reception of ofdm signals. *IEEE Transactions on Consumer Electronics*, 47:313–318.

Seo, H.-M., Woo, C.-G., and Choi, P. (2003). Relationship between ADC performance and requirements of digital-IF receiver for WCDMA base-station. *IEEE Transactions on Vehicular technology*, 52(5):1398–1408.

Snelgrove, W.M. and Sedra, A.S. (1978). Optimization of dynamic range in cascade active filters. In *IEEE International Symposium on Circuit and Systems*, pages 151–155.

Srinivasan, K. et al. (2006). Linear-programming-based techniques for synthesis of network-on-chip architectures. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 14(4):407–420.

Staszewski, R.B. et al. (2004). All-digital TX frequency synthesizer and discretetime receiver for bluetooth radio in 130-nm CMOS. *IEEE Journal of Solid-State Circuits*, 39(12):2278–2291.

Svitek, R. and Raman, S. (2005). DC offsets in direct-conversion receivers: characterization and implications. *IEEE Microwave Magazine*, 6(3):76–86.

Tafazolli, R. (2004). *Technologies for the Wireless Future: Wireless World Research Forum (WWRF)*. Wiley New York.

Tsividis, Y., Krishnapura, N., Palaskas, Y., and Toth, L. (2003). Internally varying analog circuits minimize power dissipation. *IEEE Circuits and Devices magazine*, 19(1):63–72.

Tsividis, Y.P. and Voorman, J.O. (1993). *Continuous-time analog integrated filters*. IEEE Press, New York.

Tsividis, Y.P. (1994). Integrated continuous-time filter design – An overview. *IEEE Journal of Solid-State circuits*, 29(3):166–176.

Tsividis, Y.P., Banu, M., and Khoury, J. (1986). Continuous-time MOSFET-C filters in VLSI. *IEEE Journal of Solid-State circuits*, 21(2):15–30.

Tsukutani, T. et al. (1996). Current-mode biquad without external passive elements. *IEEE Electronics Letters*, 21(18):197–198.

Tubbax, J., Come, B., der Perre, L. Van, Deneire, L., Donnay, S., and Engels, M. (2003). Compensation of IQ imbalance in OFDM systems. In *IEEE International Conference on Communications*.

Tuttlebee, W.H.W. (2002). *Software Defined Radio: Enabling Technologies*. Wiley New York.

Valkama, M., Renfors, M., and Koivunen, V. (2001). Advanced methods for I/Q imbalance compensation in communication receivers. *IEEE Transactions on Signal Processing*, 49:2335–2344.

Van Spengen, M. (2004). *MEMS reliability. Stiction, charging, and RF MEMS*. Ph.D. thesis, Katholieke Universiteit Leuven.

Vaughan, R.G., Scott, N.L., and White, D.R. (1991). The theory of bandpass sampling. *IEEE Transactions on Signal Processing*, 39(9):1973–1984.

Vejlgaard, B.N., Mogensen, P., and Knudsen, J.B. (1999). Performance analysis for UMTS downlink receiver with practical aspects. In *IEEE Vehicular Technology Conference*, pages 998–1002.

Walden, R.H. (1999). Analog-to-digital converter survey and analysis. *IEEE Journal on selected areas in communications*, 17(4):539–550.

Wolf, W. (2005). Building the Software Radio. *IEEE Computer*, 38(4):87–89.

Woonyun, K. et al. (2005). A single-chip dual-band direct-conversion IEEE 802.11a/b/g WLAN transceiver in 0.18μm CMOS. *IEEE Journal of Solid-State circuits*, 40(9):1932–1939.

Woonyun, K. et al. (2006). A direct conversion receiver with an IP2 calibrator for CDMA/PCS/GPS/AMPS applications. *IEEE Journal of Solid-State circuits*, 41(7):1535–1541.

Yoshida, H., Otaka, S., Kato, T., and Tsurumi, H. (2000). A software defined radio receiver using the direct conversion principle: implementation and evaluation. In *IEEE Intl. Symp. Personal, Indoor and Mobile Radio Communications*, 2:1044–1048.

Yuan, J. (2000). A charge sampling mixer with embedded filter function for wireless applications. In *International Conference on Microwave and Millimeter Wave Technology*, Beijing, China, pages 315–318.

Zanariadis, T.B. (2004). Migration toward 4G wireless communcations. *IEEE Wireless Communications*.

Index

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